

DEVELOPMENT OF HIGH PERFORMANCE PHOTORECEIVERS USING
GaAs-ON-Si AND $\text{In}_{0.4}\text{Ga}_{0.6}\text{As}$ -ON-GaAs MATERIAL SYSTEMS

BY

ANDREW YEN-CHANG TZENG

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TABLE OF CONTENTS

	Page
ACKNOWLEDGEMENTS	ii
ABSTRACT	vi
CHAPTERS	
1 INTRODUCTION	1
1.1 Motivation and Objectives	1
1.2 Lattice Mismatch Material Systems	3
1.3 Scope of the Present Work	6
2 LITERATURE REVIEW AND THEORETICAL BACKGROUND	10
2.1 Review of the Literature	11
2.2 Important Parameters	14
2.2.1 Transport Parameters	15
2.2.1.1 Drift parameters	15
2.2.1.2 Diffusion parameters	18
2.2.2 Band-structure Parameters	18
2.3 Photodetectors	19
2.3.1 Figures of Merit	19
2.3.2 Schottky Barrier Photodiode	22
2.3.3 p-i-n Photodiode	23
2.4 Transistors	23
2.4.1 GaAs MESFET	23
2.4.2 Si Bipolar Junction Transistor	25
3 DEVELOPMENT OF DEVICES USING GaAs-ON-Si MATERIAL SYSTEM	28
3.1 Introduction	28
3.2 GaAs Schottky Barrier Photodetector on Si Substrate	28
3.2.1 Device Design	29

	3.2.2 Thermal Superlattice and Device Fabrication	31
	3.2.3 Experiment and Results	32
	3.3 GaAs MESFET on Si Substrate	34
	3.3.1 Metal Contact	34
	3.3.2 MESFET Fabrication	35
	3.3.3 Integration of Photodiode with MESFET	36
	3.4 Conclusion	37
4	OPTIMIZATION OF GaAs/Al _{0.3} Ga _{0.7} As HIGH-SPEED SCHOTTKY BARRIER PHOTODIODE	55
	4.1 Introduction	55
	4.2 Optimization of Photodiode Design by a Scattering Matrix Technique	57
	4.2.1 Scattering Matrix Technique	57
	4.2.2 Application of Scattering Matrix Technique to the Photodiode Design	58
	4.3 Experiment and Results	60
	4.4 Conclusion	61
5	DESIGN AND ANALYSIS OF MULTI-GIGAHERTZ Si BJT PREAMPLIFIER	71
	5.1 Introduction	71
	5.2 Design of Multi-gigahertz BJT Preamplifier	71
	5.2.1 Amplifier for Capacitance Source	72
	5.2.2 Noise Estimation	75
	5.3 Simulation and Analysis	76
	5.3.1 High Performance Bipolar Technology	76
	5.3.2 Simulation and Analysis	77
	5.4 Conclusion	79
6	DEVELOPMENT OF PHOTODIODE USING In _{0.4} Ga _{0.6} As/GaAs MATERIAL SYSTEM	92
	6.1 Introduction	92
	6.2 Device Quality InGaAs Layer Grown on GaAs	92
	6.3 In _{0.4} Ga _{0.6} As p-i-n Photodiode	94
	6.3.1 Device Structure and Design	94
	6.3.2 Results and Discussion	95
	6.4 Electrical Characterization of the In _{0.4} Ga _{0.6} As Photodiode	97
	6.4.1 Generation Lifetime and Deep Level Defects	98
	6.4.2 Experiments and Discussion	99
	6.5 Conclusion	100

7	CONCLUSIONS AND RECOMMENDATIONS	114
	REFERENCES	117
	BIOGRAPHICAL SKETCH	124

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DEVELOPMENT OF HIGH PERFORMANCE PHOTORECEIVERS USING
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By

Andrew Yen-Chang Tzeng

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This work deals with the design, fabrication, and characterization of high-speed photodiodes and receivers on lattice-mismatched material systems, such as GaAs-on-Si and $\text{In}_{0.4}\text{Ga}_{0.6}\text{As}$ -on-GaAs. It consists of two parts. In the first part, the development of a high-speed Schottky barrier photodiode and receiver for the $0.8\text{ }\mu\text{m}$ wavelength detection using the GaAs-on-Si material system are described. In the second part, the development of a high performance p-i-n photodiode for the $1.3\text{ }\mu\text{m}$ wavelength detection using the $\text{In}_{0.4}\text{Ga}_{0.6}\text{As}$ -on-GaAs material system is presented.

In the development of a high-speed GaAs Schottky barrier photodiode on Si substrate, a thermal strained superlattice (TSL) structure has been used to reduce the dislocation density caused by large lattice mismatch between GaAs and Si. A reverse-biased dark current of $9 \times 10^{-10}\text{ A}$ at -5 V was achieved for the photodiode. The responsivity and quantum efficiency of the photodiode were 0.25 A/W and 42% at $0.84\text{ }\mu\text{m}$ wavelength, respectively. The response speed of the photodiode was measured to be greater than 5 GHz . The results have proved the effectiveness of incorporating the TSL structure as a buffer layer to eliminate the upward propagation of

dislocation into the device active layer. To improve the quantum efficiency-bandwidth product of the GaAs Schottky barrier photodiode, a new photodiode design using a GaAs/AlGaAs multi-layer reflector has been studied. With the aid of the multi-layer reflector, a 30% increase of responsivity has been observed in this detector while the same response speed can be retained.

In the development of an $\text{In}_{0.4}\text{Ga}_{0.6}\text{As}$ p-i-n photodiode on the GaAs substrate, a multistage scheme has been used to reduce the defects in the $\text{In}_{0.4}\text{Ga}_{0.6}\text{As}$ layer. In this technique the increment of indium content is kept below the limit of 18%, but the manipulation is repeated to achieve the desired high indium content. A responsivity of 0.45 A/W and a dark current of 5×10^{-9} A at -5 V for a 1.3 μm wavelength was achieved in this detector. The generation lifetime profile in the i-region of the photodiode was determined by the differential capacitance-voltage (C-V)/current-voltage (I-V) technique. An electron trap near the midgap of the $\text{In}_{0.4}\text{Ga}_{0.6}\text{As}$ active layer was detected by using the deep level transient spectroscopic (DLTS) measurement. The average generation lifetime derived from the DLTS measurement is consistent with the profile measurement by the I-V/C-V differential method.

To design a preamplifier for the photodetector, simulation of a multi-gigahertz Si bipolar junction transistor was carried out. The results show that a bandwidth of 2.5 to 7 GHz can be achieved depending on the value of the photodiode capacitance. The input equivalent noise current of the preamplifier was estimated to be 75 nA at 4 GHz bandwidth. Based on the results obtained from the study of photodiodes and preamplifier, a photoreceiver with a sensitivity of -28 dBm at 10^{-9} bit error rate and 45 dB dynamic range was obtained.

CHAPTER 1 INTRODUCTION

1.1 Motivation and Objectives

The importance of using optical means for data transmission and processing is well recognized by many for its advantages such as transmission speed and distance, freedom from electromagnetic noise, low interchannel cross talk, freedom from grounding and impedance-matching problems, small size, and light weight. Photodetectors fabricated from III-V compound semiconductor materials have been the key component in the realization of various optical communication and signal processing systems. The data rate in these systems has exceeded 1 G bit/s^1 and will soon be in the several gigabit range. However, the use of conventional discrete optoelectronic components will limit the speed, due to parasitics introduced in the assembly processes. Thus, there is a need to improve system performance not only in speed, but also in a variety of directions. The multichannel signal-handling capability is one direction; transmitting, switching and processing data to and from many-signal channels are indispensable for constructing large-capacity systems with high diversity. Furthermore, packaging of discrete optoelectronic components with other electronic circuits cannot be done in the batch-type method and, hence, is not easily scaled up for mass-production. Monolithic integration of optoelectronic integrated circuits (OEICs) can overcome these problems. Therefore, it has a greater potential to reduce the per channel cost for fiber-optic data communication.

To make photonic devices useful in system construction, many other electronic device components should be integrated with photonic devices. In particular, several electronic circuits must be interconnected to the system without introducing any

degradation on device performance. For instance, a photodetector must be followed by a preamplifier, a signal-precondition circuit and a signal-processing circuit accepting an external control signal. Thus, the idea is to integrate optical devices and electronic circuits monolithically on a single semiconductor substrate.²⁻⁴ The most ambitious goal of research and development on OEICs is to develop a practical technology that can integrate both the passive optical elements and active optical elements, such as waveguide, photodetectors, optical source (lasers and LEDs), and active electronic circuits, together on a single chip. Since each of these elements requires different materials characteristics and processing procedures, much of the work to date⁵ has been focused on development of discrete components.

In the development of various electronic and optical components, it is obvious that Si is the most widely used material for electronic circuits due to its maturity in both bipolar and complementary metal-oxide-semiconductor (CMOS) technologies. The CMOS circuits have found many applications in optoelectronic data communication due to its low power consumption advantage.⁶ The GaAs/AlGaAs material system has been extensively developed as lasers and detectors for short wavelength (0.8- μm) communication.⁷ In the 1.3- or 1.55- μm wavelength region, sources and detectors are made on the InGaAs/InP material system for wide-band optical fiber communications.¹ It is highly desirable to integrate source, detector, and electronic components from different material systems into an optoelectronic circuitry on the same substrate. Nevertheless, the hetero epitaxy of GaAs on Si and/or $\text{In}_x\text{Ga}_{1-x}\text{As}$ (with $x > 0.4$) on GaAs faces a serious lattice mismatch problem. This obstacle prevents the successful fabrication of high quality GaAs photonic devices on Si substrate (for 0.8- μm) and $\text{In}_x\text{Ga}_{1-x}\text{As}$ ($x > 0.4$) devices on GaAs substrate (for 1.3- and 1.55- μm). This in turn prevents the large-scale integration of the mature elements using a different material system. Therefore, the goal of this research is to develop high quality photonic devices on the lattice-mismatched material system for both near in-

frared ($0.8\text{-}\mu\text{m}$) and longer wavelength (1.3- or $1.55\text{-}\mu\text{m}$) applications. For the $0.8\text{ }\mu\text{m}$ wavelength application, the GaAs-on-Si material system was chosen for this study. An innovative GaAs photodiode was successfully developed on this material system, which can be monolithically integrated with the Si electronic circuits on the same chip. For the $1.3\text{ }\mu\text{m}$ wavelength, the $\text{In}_{0.4}\text{Ga}_{0.6}\text{As}$ -on-GaAs material system was investigated. An $\text{In}_{0.4}\text{Ga}_{0.6}\text{As}$ p-i-n photodiode was developed on this material system. For a complete receiver design, a low noise preamplifier is indispensable. Therefore, the design and analysis of a wide-bandwidth and low noise Si bipolar junction transistor (BJT) preamplifier is included.

1.2 Lattice Mismatch Material Systems

Following the demonstration of infrared lasers from lead salt compounds at low temperature⁸ and the continuous operation of GaAs heterojunction lasers in 1969,⁹ there has been a steadily growing interest in material systems involving heterostructures between different semiconductors. In order to minimize the strain and dislocations associated with lattice mismatch, the difference in lattice parameter between the heterostructure constituents of these material systems is usually less than 0.1%.¹⁰ When the lattice parameter mismatch exceeds 1%, the nucleation of a film on a substrate of different compositions by liquid-phase epitaxy (LPE) is difficult. However, using molecular-beam epitaxy (MBE), extended planar layering can still be achieved with lattice mismatch as large as 4%. In this research, we demonstrate the capability of using the MBE technique to develop two device quality material systems, GaAs-on-Si substrate and $\text{In}_{0.4}\text{Ga}_{0.6}\text{As}$ -on-GaAs substrate, which have large lattice mismatch of 4.1% and 2.8%, respectively. The important factors which affect the growth of lattice-mismatched material systems are compared in Table 1.1 for these two specific material systems.

The basic principle of strained-layer epitaxy is that a certain amount of elastic strain can be accommodated by any material without generating dislocations or de-

fects. Whereas this statement may appear trivial on the macroscopic level, it also applies to crystal growth on the atomic level. It takes energy to accommodate an epitaxial layer of lattice mismatched material. The energy depends on both the thickness and the size of the lattice mismatch. On the other hand, it also takes energy to create a dislocation that can relieve the lattice mismatch strain. If the thickness of the epitaxial layer is kept low enough to maintain the elastic strain energy below the energy of dislocation formation, the strained-layer structure will be thermodynamically stable against dislocation formation. Obviously, the unstrained state of the lattice-mismatched layer is energetically most favorable. However, the strained structure is stable against transformation to the unstrained state by the energy barrier associated with the generation of enough dislocations to relieve the strain.¹¹ The idea of a critical thickness beyond which the energy required to accommodate elastic strain exceeds the fixed energy of dislocation formation was then further developed and quantified by Matthews and Blakeslee.¹²

The treatment by Matthews and Blakeslee¹² has found wide application to a number of strained systems. In this model, the critical thickness h_c depends on the lattice parameter mismatch or strain ε and the magnitude of the Burgers vector b for slip dislocation

$$h_c = \left(\frac{1}{\varepsilon}\right) \left[\frac{b(1 - \nu \cos^2 \theta)}{8\pi(1 + \nu) \cos \lambda} \right] [\ell_n(4h_c/b)] \quad (1.1)$$

where

ν = Poisson's ratio, calculated from the elastic constant

θ, λ = angles between the slip planes and the crystal surfaces.

Therefore, in the InGaAs/GaAs material system, proper adjustment of the indium content in each growth stage and control of the thickness of each buffer layer to meet the critical thickness requirement will result in a low dislocation InGaAs layer for device fabrication.

However, in the GaAs/Si material system, the difference in the lattice parameter

is greater than 4%, which is much larger than that in the InGaAs/GaAs system. To achieve a low-dislocation device quality growth on Si substrate, it is necessary to apply additional techniques besides the control of the layer critical thickness. In the GaAs/Si system, one additional nature is that the thermal expansion coefficient in GaAs is 60% larger than that of Si. By using this characteristic, several researchers¹³⁻¹⁵ have developed a thermal cycle growth technique, which is also known as the thermal strained superlattice (TSL) technique. In this technique, shown in Fig. 1.1, a GaAs buffer layer was first deposited at a higher temperature (usually 525°C) on Si substrate. After the growth ceased, the layer is low strained but with high dislocation density. Next, the growth temperature was lowered to 400°C. The lattice constant of the new grown layer is smaller than those grown at 525°C since the thermal shrinkage in Si is much smaller than in GaAs. This in turn limits the previous grown GaAs layer to shrink to the size of lattice constant at 400°C. Thus, the interface structure between the two GaAs layers grown at different temperatures will experience tension, which in turn causes strains within the layers to offset the tension. Next, the growth temperature increased to 665°C. By similar argument, but now in the opposite direction, the new grown layer interface will experience compression. And the strain is generated within the new grown layers to cancel the compression. The alternative tension-compression changing force and the subsequent strain generation or relief tend to force the movement of dislocation within the material toward edge and interface. Yamaguchi et al.¹⁶ proposed a simple model to analyze the dislocation annihilation and reemission due to the thermal cycling effect.

$$D \xrightarrow{K_1} \text{annihilation}, \quad (1.2)$$

$$D + D \xrightarrow{K_2} D_2, \quad (1.3)$$

where D and D_2 are densities of dislocations and coalesced dislocation, respectively, K_1 and K_2 are the corresponding rate constants.

The reaction equations for dislocations (D) are given by

$$\frac{dD}{dt} = -K_1 D - K_2 D^2 \quad (1.4)$$

$$\frac{dD_2}{dt} = \frac{K_2 D^2}{2} \quad (1.5)$$

Here, Eq. (1.4) shows dislocation annihilations such as deflection to edge and interface, and coalescence, and Eq. (1.5) shows reemission after coalescence. The initial conditions are given as $D=D_0$, $D_2=0$, at $t=0$. The resulting solutions are given by

$$D = \frac{1}{(1/D_0 + K_2/D_1)\exp(K_1 t) - K_2/K_1}, \quad (1.6)$$

and

$$D_2 = (D_0^2 K_2 / K_1) \{1 - [\exp(-K_1 t)]^2\} \quad (1.7)$$

respectively.

1.3 Scope of the Present Work

This thesis is organized into seven chapters. In Chapter 1, a statement of the motivation and objectives of this study is presented. The problems and features of the lattice-mismatched material systems are also addressed.

Chapter 2 reviews the status, the theoretical background and considerations for the design of high speed photonic devices and receivers.

In Chapter 3, the successful development of a high speed GaAs/Al_{0.3}Ga_{0.7}As Schottky barrier photodiode and a high-transconductance GaAs MESFET grown on Si substrate is described. In addition, results of a simple hybrid integration of photodiode with MESFET on a 50 Ω microstrip line are discussed.

In Chapter 4, the application of the scattering matrix technique to the photodiode design for the optimization of the efficiency-speed product is presented. A novel multi-layer reflector GaAs/Al_{0.3}Ga_{0.7}As Schottky barrier photodiode has been developed

by using this design approach to improve quantum efficiency of the photodiode while retaining wide bandwidth.

In Chapter 5, the design of a multi-gigahertz Si preamplifier by using the latest double-poly self-aligned BJT technology is described. The circuit simulation results, an analysis of the stability of the circuit, and the performance of the amplifier circuit are presented. Noise analysis of the designed circuit is also included.

In Chapter 6, we report the successful development of a low leakage current, planar $\text{In}_{0.4}\text{Ga}_{0.6}\text{As}$ p-i-n photodiode grown on GaAs substrate. The different growth schemes of strain-relief layer are compared. The electrical characterization of the generation lifetime in an InGaAs/GaAs p-i-n photodiode by the differential I-V/C-V method is discussed. A deep level transient spectroscopy (DLTS) study of the deep level defects in this device is also included.

In Chapter 7, the results and achievements of this research are summarized. Based on the findings of this work, suggestions and recommendations for further study are presented.

Table 1.1 Comparison of the GaAs-on-Si and $\text{In}_{0.4}\text{Ga}_{0.6}\text{As}$ -on-GaAs lattice-mismatched material systems.

	GaAs/Si	$\text{In}_{0.4}\text{Ga}_{0.6}\text{As}/\text{GaAs}$
Difference on lattice parameter	4.1 %	2.8 %
Difference on thermal expansion coefficient	60 %	10 %
Growth initiation	non-polar to polar	polar to polar
Stiffness of material	$\text{Si} > \text{GaAs}$	$\text{In}_{0.4}\text{Ga}_{0.6}\text{As} > \text{GaAs}$
Defect reduction technique	TSL	strain-relief buffer

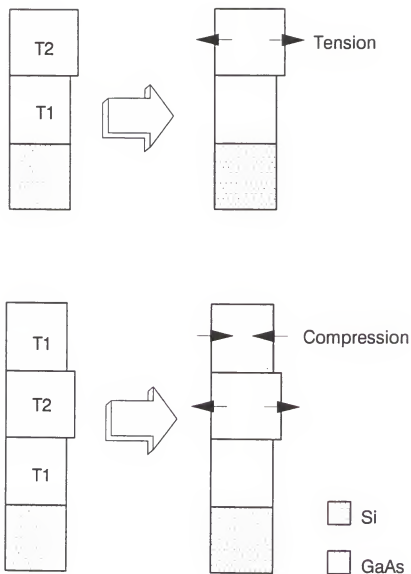


Figure 1.1 Thermal strained superlattice (TSL) growth scheme of the GaAs-on-Si material growth.

CHAPTER 2

LITERATURE REVIEW AND THEORETICAL BACKGROUND

High-speed devices are used to perform many analog and digital functions, including linear signal amplification, modulation or demodulation, or simple on-off switching in computers. They can generally switch on or off in a picosecond or even less. As system requirements increase the speed at which these devices must operate, their sizes necessarily decrease, and effects previously considered of second order now become important. For instance, the hot electron effect that can occur at high electric fields existing in very small devices can lead to severe performance and reliability problems. Therefore, it becomes necessary to understand the detailed physics of operating these high-speed devices.

Photonic devices such as photodetectors (which convert radiation into electrical voltages or currents), LEDs and lasers (which emit optical radiation), and modulators (which invert the propagation of light by applying electric fields) are used primarily for optical communications, signal processing, optical computing, and interconnect applications. Demands for speed, sensitivity, and increased signal-to-noise ratio for these devices also increase continuously. In this study, we only focus our efforts on the photodetector and its integration with GaAs MESFETs and Si BJTs.

In this chapter, we first present a literature review of the development of photoreceivers, recent development of their related devices, and development of the photonic devices on lattice-mismatched material systems. Next, we discuss the parameters which, in general, determine various aspects of the operation of high-speed electronic and optoelectronic devices. The devices of interest are described, and the ways in which these parameters affect them are explained.

2.1 Review of the Literature

The design of a photoreceiver for an optical-fiber transmission system has been reported by several researchers in a number of papers,^{17–20} mostly by Personick, who in his pioneering work formulated the theoretical analysis. Most of these papers are concerned with telecommunication applications. Receiver design for telecommunications is based on a variety of system design considerations, including sensitivity, bandwidth and dynamic range. Sensitivity is a measure of the minimum optical power level required at the receiver input so that it will operate reliably with a bit error rate less than a desired value. Bandwidth defines the maximum operating rate of the receiver. Furthermore, in practical systems a receiver has to operate not only at the minimum detectable power but also at an optical power level which can be significantly large. Therefore, the receiver dynamic range is defined as the difference (in decibels) between the minimum detectable power level, i.e., receiver sensitivity, and the maximum allowable input power level. All these three photoreceiver characteristics are interrelated, sometimes even conflicted. Receiver design requirements for digital telecommunications as well as local data communications have been discussed by Personick.²¹ A detailed discussion of the different requirements and design tradeoffs between conflicting receiver requirements were given by Muoi.¹

All these early works are based on the technology of discrete-device circuit design. Due to the large stray capacitance and inductance in the circuits, the bandwidth of the receiver is relatively small. To accommodate a good sensitivity, the input impedance of the front-end amplifier needs to be high. This in turn integrates the pulse input signal, and additional equalizing circuit is needed to restore the input signal. Recently, a 400 Mbit (Si BJT) to 4 Gbit/s (GaAs MESFET) single-chip optical preamplifier has been reported.^{22–24} However, the photodiodes used in these receivers are still discrete devices, which are hybrid-mounted to the preamplifiers.

For an optimized FET front-end receiver, a sensitivity figure of merit²⁵ was stated

to be the quantity g_m/C_T^2 , where g_m is the input FET transconductance and C_T is the total input capacitance for an FET front-end. This similar figure of merit was given as β/C_T for the case of BJT, where β is the current gain of transistor. In either case, the reduction of input parasitic capacitance is desirable. Secondly, parasitic inductance becomes very important at multi-gigahertz bandwidth. For instance, a single $200\mu\text{m}$ -long, $18\mu\text{m}$ -wide wire band will represent approximately $0.2\mu\text{m}$ of inductance. At 10GHz this corresponds to 12.5Ω of series impedance. At the same frequency, 1pF of input parasitic capacitance represents 16Ω of input impedance. In a hybrid approach, the combination of parasitic inductance and capacitance can translate to as much as 2.5dB of extra optical sensitivity loss. Therefore, monolithic integration of photonics and electronics for optical fiber communication has been predicted to enjoy a much higher sensitivity.²⁶

Experiments with optoelectronic integration began when Lee et al.²⁷ integrated a semiconductor laser and a Gunn effect logical element on a single GaAs substrate. Later, several workers had shown the feasibility of monolithic integration of PIN/FET photoreceivers.^{28–30} An obstacle to the successful integration of the FET (a planar device) and the PIN photodiode (a vertical device) is the incompatibility of the device structure and fabrication process. To resolve the problem, Sussman and his coworkers³¹ first demonstrated a high-performance, flip-chip integrated p-i-n/amplifier receiver by using a back-illuminated, small-junction InP/InGaAs p-i-n photodiode and a GaAs amplifier. Later, in Wada and his coworker's work³² a gigabit-per-second rate flip-chip receiver with high sensitivity has been achieved by using a similar device combination. Another approach to avoiding the obstacle is using an MSM photodiode instead of a p-i-n photodiode. Ito et al.³³ first reported the monolithic integration of an MSM-PD and a GaAs preamplifier (FET). Later in several other works,^{34–36} using this type of detector, optical receivers have been fabricated on integrated circuits which contain as many as 1200 logic gates and have demon-

strated sensitivities comparable to that of the state-of-the-art hybrid design. In the latest development, Ewen et al.³⁷ have successfully fabricated a 4-channel receiver array with bandwidth of >1 Gb/s performance in the development of a fiber-optic data communication link on GaAs substrate. The receiver IC consists of an array of four receivers, a phase lock loop (PLL) retiming circuit, and a 1:10 deserializer circuit. It contains approximately 8000 devices, operates up to 1 Gb/S, and nominally dissipates 800 mW.

Using Si bipolar ICs for lightwave communications in the multigigabit-per-second range, Rein³⁸ has pointed out the possible role of Si IC in this area due to its technological maturity and volume industrial production. In a typical digital optical-fiber transmission system, the preamplifier and laser driver are the most difficult circuit components to be realized by the Si BJT technology due to the low-noise requirements and high-output-current swing, respectively. In this research our interest is mainly concentrated on the former. Recent results in the development of preamplifier IC by using advanced double-poly self-aligning technologies (Discussion of the technology will be given in Chapter 4) were reported by Hamano et al.³⁹ and by Fujita et al.⁴⁰ The former has a transimpedance of 468 Ω and a cut off frequency of 3.6 GHz. The latter shows an input sensitivity of -31.8 dBm at 5 Gb/s.

From the above review, it is seen that two types of the monolithic OEICs have been developed so far. The GaAs OEIC uses GaAs substrate and has been studied for short wavelength (0.8-0.9 μm) systems. On the other hand, the InP-based OEIC is the choice for long wavelength (1.3-1.6 μm) systems. Nevertheless, the integration of GaAs photodiodes with the Si electronic elements or the integration of InGaAs optical devices with GaAs (or Si) electronic elements is only seen in the hybrid system due to the difficulty of the lattice mismatch properties (see Table 1.1) between these materials.

To tackle the problems of growing device quality GaAs on Si substrate, Gale

et al.⁴¹ did the pioneering work by growing successfully the device quality GaAs on a Ge thin film which was in turn grown on a Si substrate. Followed this breakthrough, research work on development of GaAs photonic devices on Si substrate has sprouted.^{42–45} For the photodetector developed on GaAs substrate, avalanche photodiode was reported by Chand et al.⁴⁶ with a gain of 7 at -10V. Interdigitated metal-semiconductor-metal (IMSM) detector was reported by Adkisson et al.⁴⁷ with a 4 GHz bandwidth but poor responsivity. A p-i-n photodiode was done by Paslaski et al.⁴⁸ with greater than 4GHz bandwidth but a relatively large dark current of 100 nA. GaAs photoconductor formed on Si substrate has also been reported by More et al.⁴⁹

For the InGaAs photonic devices fabricated on GaAs substrate, the pioneer work was done by Nahory et al.⁵⁰ They successfully fabricated a 1.3 μm LED on GaAs by using liquid phase epitaxial growth technique. Later, using MBE and MOCVD growth techniques, new results have been reported consecutively.^{51–53} In the development of InGaAs photodiode on GaAs substrate, Denti et al.⁵⁴ reported a p-i-n diode on $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}/\text{InP}/\text{GaAs}$ wafer by MOCVD growth. Their device showed a bandwidth of greater than 4GHz but a relatively poor responsivity. More recently, Rogers et al.⁵⁵ reported a high-speed IMSM detector fabricated on semi-insulating GaAs substrate using two GaInAs layers of different indium content to accommodate most of the lattice mismatch via interface misfit dislocations. Their device showed a 3 GHz bandwidth but with very large leakage current.

2.2 Important Parameters

Depending on the acceptable level of approximation used in the analysis of any devices, definitions of material and device parameters may vary. Choice of the appropriate definition will depend on the dimensions of the device under study, electric fields within, and time scales. For example, in describing carrier transport the parameters at various levels can be divided as: 1) hydrodynamic equation level, 2) semiclassical

transport level. 3) quantum transport level. The first one is useful for describing conventional devices in which electric fields do not exceed the value at which mobility is no longer a constant. The last one includes the interference among carriers and the coupling effect of intervalley scattering. It is the most accurate carrier transport description, but its calculation involves very complicated mathematical manipulation. Thus, the second level seems appropriate for describing devices in which high-field effects are significant.

Because of the need to reduce parasitic capacitance, the higher the speed at which devices must work, and the smaller they must be. Furthermore, since signal-to-noise must be maintained in the existence of power-supply transients, operating voltage levels cannot easily be reduced as device size is reduced. Therefore, peak electric fields inside devices inevitably increase as speeds are increased, and proper understanding of high-speed devices requires that material and device parameters be specified to at least the second level, which includes the hot electron effect.

Both the transport parameters and band-structure parameters affect the performance of high-speed optoelectronic devices. The former may be considered direct determinants of switching times or maximum frequency of amplification or detection. The latter affect both carrier transport and optical frequency in which the device of interest responds.

2.2.1 Transport Parameters

2.2.1.1 Drift parameters

A majority-carrier device is one in which the switching performance depends on the transport of majority carriers. For example, a field-effect transistor is a majority-carrier device. In the total depleted i-region of a p-i-n diode, since the free carriers do not exist, the transport behavior of electron-hole pairs generated by the incident photons is determined by the drift velocity. The speed with which a majority-carrier device operates is primarily determined by the transit time of carriers across some

modulation length,⁵⁶

$$t = L / \langle v \rangle \quad (2.1)$$

where t is a measure of switching speed or inverse of some maximum frequency of amplification, L is the active length of the device, and $\langle v \rangle$ is the average carrier drift velocity across the active length.

For minority carriers, the electron or hole drift velocity v can be related to the applied electric field ε as

$$v = \mu \varepsilon \quad (2.2)$$

where μ is the carrier mobility. However, the approximation that mobility is a constant is not good enough to describe the behavior of high-speed devices, in which electric fields may reach values in excess of 10^5 V/cm. To simplify device analysis, empirical formulas are often used to express the variation of mobility with temperature, impurity concentration, field, and field anisotropy. These curve-fitting formulas which are at the second level of approximation, specify that:

$$\mu = q\tau/m^* \quad (2.3)$$

where q is electronic charge, m^* is the carrier effective mass, and τ is the average relaxation time. The effective mass, if properly described as a tensor function of electron energy, is a shorthand description of the band structure. If there is more than one scattering process, and all may be described by a relaxation time, then the overall average relaxation time is obtained from

$$\frac{1}{\tau} = \sum_{i=1}^n \frac{1}{\tau_i} \quad (2.4)$$

Here in our material system, τ_i may include the relaxation time of several different scattering processes as shown in the following expressions⁵⁷:

For acoustic phonon scattering in GaAs central valley,

$$\frac{1}{\tau_a} = \frac{\sqrt{2}}{\pi} \frac{E_i^2 m^{*3/2} K T}{\hbar^4 p c_1^2} E^{1/2} \quad (2.5)$$

For polar optical phonon scattering,

$$\frac{1}{\tau_{po}} = \frac{q^2 \omega_1}{4\sqrt{2\pi\epsilon}} \left(\frac{1}{k_\infty} - \frac{1}{k_1} \right) \frac{m^{*1/2}}{\hbar\sqrt{E}} (2n_o + 1) \quad (2.6)$$

For intervalley phonon scattering,

$$\frac{1}{\tau_{jo}} = \sum_i^{i \neq j} \frac{(2m_D)^{3/2}}{4\pi\hbar^3\rho} \frac{D_{ji}^2}{\omega_{ji}^2} [n_j(E + \hbar\omega_{ji})^{1/2} + (n_j + 1)(E - \hbar\omega_{ji})^{1/2}] \quad (2.7)$$

For ionized impurity scattering

$$\frac{1}{\tau_{ii}} = \frac{Z^2 q^4 N_i C}{16\pi(2m^*)^{1/2}\epsilon^2} E^{-3/2} \quad (2.8)$$

In the preceding expressions, the symbols are:

E = total electron energy

q = electronic charge

k = Boltzmann constant

h = Planck constant

$\hbar = \frac{h}{2\pi}$

ρ = density

C_1 = acoustic velocity

ϵ = dielectric constant

K_∞, K_1 = high- and low-frequency dielectric constant, respectively

m^*, m_D = density of states effective mass and free electron mass

n_o = number of optical phonons

n_j = intervalley phonon density

ω_o = optical phonon frequency

ω_{ij} = frequency of ij intervalley phonon

D_{ij} = intervalley scattering deformation potential

N_i = scattering centers/unit volume

C = a constant, $1.4 < C < 2$

$Z = 1$ for single charged impurity etc.

2.2.1.2 Diffusion parameters

Carrier transport by diffusion is related to relaxation of a distribution function, as is in the drift case. For carrier concentrations that are small compared to the density of conduction or valence band states and at low fields, the relationship between the mobility and diffusion constant is given by Einstein relation:

$$D = \mu kT/q \quad (2.9)$$

where D is the diffusion coefficient, μ is carrier mobility and T is temperature.

2.2.2 Band-structure Parameters

The band structure of a crystalline solid⁵⁸ relates the energy E of charge carriers to their momentum ($\hbar k$) and is determined by setting up the corresponding Schrödinger's equation for the solid of interest and solving it. For all semiconductors, there are regions in the E - k plane in which solutions do not exist. The difference in energy between the maximum energy of the highest allowed energy band filled with carriers at 0K (the valence band) and the minimum energy of the next allowed band above it (the conduction band) is called the energy gap.

The energy gap is an important semiconductor parameter. The optical frequencies for light detection as well as emission are determined by this parameter. For ternary compound semiconductors such as $\text{In}_{1-x}\text{Ga}_x\text{As}$ in our case, the energy gap can be changed by adjusting the value of composition ratio, x . In fact, the bandgap of the $\text{In}_{1-x}\text{Ga}_x\text{As}$ material can be calculated by using the following empirical formula⁵⁹:

$$E_g(x) = 0.36 + 0.505x + 0.555x^2 \quad (2.10)$$

Thus, by changing the composition ratio during the material growth, we can adjust the bandgap value to fit the desired optical wavelength (e.g., 1.3 and 1.5 μm for fiber optical communication).

In addition, when the lattice of solid experiences anisotropic deformation, the band structure will also be changed. In a semiconductor, the biaxial stress can split

the valence band degeneracy.⁶⁰ For GaAs on Si, the split causes a change in the transition energy between the conduction band and the heavy/light hole valence bands. The difference in transition energy between the strained and unstrained transitions is calculated to be^{61,62}

$$\Delta E_{lh} = [-2a(C_{11} - C_{12})/C_{11} + b(C_{11} + 2C_{12})/C_{11}]\epsilon \quad (2.11)$$

$$\Delta E_{hh} = [-2a(C_{11} - C_{12})/C_{11} - b(C_{11} + 2C_{12})/C_{11}]\epsilon \quad (2.12)$$

where C_{ij} is the elastic stiffness coefficients, a is the hydrostatic deformation potential, and b is the shear deformation potential.

2.3 Photodetectors

In photodetectors, incident illumination of the proper photon energy creates electron-hole pairs that cause photo-current to flow in an external circuit. The process is the direct inverse of that occurring in photoemitters where current flow in an external circuit leads to recombination of electron-hole pairs with consequent photoemission. The generation of carriers by photons is a much more probable occurrence than the generation of photons by recombination of carrier pair, so that photodetectors do not need direct-gap semiconductors. To achieve the desired photodetector characteristics of high sensitivity and speed, photodetectors may be made in the form of heterostructure devices. To lower system cost and improve performance, detectors and preamplifiers may be fabricated together monolithically as optoelectronic circuits.

2.3.1 Figures of Merit

The most commonly used figures of merit for evaluating the performance of a photodiode are the quantum efficiency,⁶³ the noise equivalent power (NEP), and the detectivity (D^*). In high speed applications, such as on chip optical link, the response

speed of the photodetector is also critical. The quantum efficiency is the number of electron-hole pairs generated within the device of interest per incident photon. It can be defined as⁶⁴

$$\eta = \frac{I_{ph}}{P_{opt}\lambda} \times 124\% \quad (2.13)$$

where I_{ph} is photocurrent generated, and P_{opt} is the input optical power at wavelength λ .

The quantum efficiency η is determined at low reverse bias voltage in which no avalanche multiplication takes place. A related figure of merit is the responsivity, which is the ratio of the photocurrent to the input optical power, $R=I_{ph}/P$. This is a directly measurable quantity. The noise equivalent power (NEP) is another figure of merit widely used in assessing the performance of photodetector. By definition NEP is the incident rms optical power required to produce a signal-to-noise of one in a 1-HZ bandwidth. For a specific wavelength (which corresponds to a certain optical energy $h\nu$) of incident light, the NEP is given by

$$NEP = \frac{i_{nrms}}{R} = \frac{i_{nrms}}{I_{ph}} h\nu q \Phi \quad (2.14)$$

where

i_{nrms} = detector noise current (A)

I_{ph} = detector signal current (A)

$h\nu$ = incident photon energy in eV

Φ = the rms photon flux density required to produce $S/N=1$ (cm^{-2}/s).

Since NEP is a measurement of noise power, it depends on many parameters such as detector area, electrical bandwidth, spectral region, detector bias and responsivity.

Clark Jones et al.⁶⁵ introduced a specific detectivity “ D^* ” given by

$$D^* = \frac{\sqrt{A_d \Delta f}}{NEP} \quad (2.15)$$

where

A_d = active area of detector

Δf = the effective noise bandwidth of the detector system.

In the optical fiber communication, usually the system designers will maintain the light source level several orders of magnitude higher than the background noise limit which is the case for IR and black body radiation detection. Thus the above mentioned figures of merit NEP and D^* are not as critical as the response speed of the photodetectors for the on-chip optical link application.

The response speed of a photodetector is determined mainly by three parameters, the transit time t_{tr} across the depletion region, the diffusion time t_{dif} in the quasi-neutral region, and the RC time t_{RC} required to discharge the junction capacitance through the internal resistance. The total risetime can be expressed by

$$t_r = (t_{tr}^2 + t_{dif}^2 + t_{RC}^2)^{1/2} \quad (2.16)$$

Its corresponding 3-dB cutoff frequency, often regarded as the bandwidth of the photodiode, is given by $f_c = 0.35/t_r$.

The transit time of the photogenerated excess carriers across the depletion region is given by $t_{tr} = W/(2.8v_s)$ where v_s is given by equation (2) and W is the depletion layer width. This expression is true only for a constant junction field and for electrons injecting into the junction, but it remains a good approximation for carriers generated in the depletion region.⁶⁶ For high mobility material, the transit time is limited by the saturated drift velocity for which hot electron effect has been accounted. The carriers generated in a quasineutral region need a diffusion time delay to reach the drift region. The diffusion time is given by $t_{dif} = W_{p,n}^2/(2.43D_{n,p})$, where $W_{p,n}$ is the thickness of the p- and n-type quasi-neutral base regions, respectively.

The equivalent lumped circuit elements of a photodiode also limit its response speed. The RC time is given by $t_{RC} = (R_S + R_L)C_j$. The series resistance consists of the lead resistance, the sheet resistance of the p- and n-type quasi-neutral base region, and the metal-semiconductor contact resistance. This resistance is distributed and frequency-dependent depending on the contact geometry. The intrinsic response

speed of the photodetector is further degraded by the load resistance, parasitic capacitance, and the lead inductance due to the bounding wires. To analyze the effects of extrinsic circuit elements, a simulation result is shown in Fig. 2.1 along with an equivalent circuit.

2.3.2 Schottky Barrier Photodiode

The Schottky barrier photodiode (SBD) is also called the metal-semiconductor photodiode since its junction is formed by the rectifying Schottky barrier contact at the interface between metal and semiconductor. SBD is particularly useful in the spectral range from UV to near IR wavelength. The SBD has a very high quantum efficiency when it is operating in the depletion mode. In this case, the incident photons are absorbed inside the bulk semiconductor. Electron hole pairs are created by photons with energy greater than the bandgap energy; and the cutoff wavelength of the photodetector is determined by the bandgap energy of the semiconductor.

The total photocurrent of an n-type Schottky barrier photodiode mainly consists of two components coming from the depletion region and the quasi-neutral base region:

$$J_{ph} = q(1-R)\Phi(\lambda)(1-e^{-\alpha w}) + \frac{q(1-R)\Phi(\lambda)\alpha L_p}{\alpha^2 L_p^2 - 1} e^{-\alpha w} \times \left\{ \alpha L_p - \frac{\cosh(W_n/L_p) - e^{-\alpha W_n}}{\sinh(W_n/L_p)} \right\} \quad (2.17)$$

where

R = reflection coefficient of the SBD

α = absorption coefficient (cm^{-1})

$\Phi(\lambda)$ = the incident photon flux density at wavelength λ ($\text{cm}^{-2}\text{-s}^{-1}$)

W = the depletion layer width (cm)

W_n = the thickness of quasi-neutral base (cm).

The quantum efficiency of an SBD can be obtained by substituting equation

(2.16) into equation (2.12):

$$\eta = (1 - R) \left\{ 1 - e^{-\alpha W} \left[1 - \frac{\alpha L_n}{\alpha^2 L_p^2 - 1} \left(\alpha L_p - \frac{\cosh\left(\frac{W_n}{L_p}\right) - e^{-\alpha W_n}}{\sinh\left(\frac{W_n}{L_p}\right)} \right) \right] \right\} \quad (2.18)$$

2.3.3 p-i-n Photodiode

The p-i-n photodiode is the most common detector structure used in the visible to near IR spectral range. The reason for its popularity is that the spectral response can be tailored by adjusting the intrinsic layer thickness. A p-i-n photodiode is also operated in the depletion mode in which a sufficient reverse bias is applied to the diode to maintain a total depletion in the i-region. When photons with energy larger than the energy gap of the semiconductor are impinging upon the diode, short wavelength photons will be absorbed in the p^+ region while the majority of photons are absorbed in the i-region. Excess carriers generated in the i-region are swept out by the electric field built up by the applied bias voltage across the diode. The total photocurrent can be expressed as⁶⁴

$$J_{ph} = q\phi(\lambda)(1 - R) \left\{ \frac{1}{\alpha L_n \sinh\left(\frac{W_n}{L_n}\right)} \left[1 - \cosh\left(\frac{W_p}{L_n}\right) e^{-\alpha W_p} \right] - \frac{e^{-\alpha W}}{1 + \alpha L_p} \right\} \quad (2.19)$$

Its quantum efficiency $[=J_{ph}/q\phi(\lambda)]$ can be calculated in the same way as those of Schottky barrier detector.

2.4 Transistors

2.4.1 GaAs MESFET

MESFET is the acronym of MEtal-Semiconductor Field Effect Transistor. A field-effect transistor is a three-terminal switch or amplifier in which the flow of current from one electrode (the source) to another (the drain) either is switched on and off by a voltage applied to a third control electrode (the gate) or is modulated in a less drastic fashion by a voltage on the gate smaller than that required to fully shut off the current. Since the change in current flow to the drain (ΔI_D) depends, ideally,

only on the change in voltage on the gate (ΔV_G) and is independent of the drain voltage, voltage gain is possible. The figure of merit of a MESFET is the mutual transconductance,

$$g_m = \partial I_D / \partial V_G \quad (2.20)$$

Figure 2.2 shows the cross-sectional view of a MESFET under a simplified representation where a negative gate voltage is applied to the gate electrode, a depletion region is created under the gate in which no mobile carriers exist and the device is in the off condition. The classical analysis of a MESFET structure assumes constant mobility and neglects diffusion effect and electric field along the channel. The drain current can be expressed in terms of the drain and gate voltages and is given by⁶⁷:

$$I_D = G_o \left\{ V_D - \frac{2}{3} \left(\frac{2\epsilon_s}{N_d t^2} \right)^{1/2} [(\phi_i - V_G + V_D)^{3/2} + (\phi_i - V_G)^{3/2}] \right\} \quad (2.21)$$

where

ϕ_i = the built-in-barrier voltage at the gate (eV)

N_d = the doping density in the n-type active layer (cm^{-3})

t = the channel thickness (μm)

G_o = the conductance of the metallurgical channel (Ω^{-1}).

The speed of a field-effect transistor depends on the charging and discharging time of the device capacitance and the minimum time in which an interruption to the current in the channel can be observed at drain. The transconductance (Eq. 2.20) is a measure of the first parameter, while the transit time (Eq. 2.1) with the channel length L is a measure of the second. Both these measures indicate that the velocity of electron in the channel is the most important parameter in determining device speed. However, parasitic resistances and capacitances of the device may also influence the device speed and must not be overlooked.

2.4.2 Si Bipolar Junction Transistor

The basic equation that describes the physics of a bipolar junction transistor (BJT) action is given by⁶⁷

$$J = J_s \left[\exp\left(\frac{qV_{BC}}{KT}\right) - \exp\left(\frac{qV_{BE}}{KT}\right) \right] \quad (2.22)$$

where

$$J_s = \frac{q^2 n_i^2 D_n}{Q_s} \quad (2.23)$$

is the saturation current density, Q_s is the total majority-carrier charge per unit area in the base, n_i is the intrinsic carrier density, and D_n , the average diffusion constant, is defined by Eq. 2.9. In a BJT, the speed depends on the minority carrier transit time τ_B across the quasi-neutral base and the ability to increase the current available to drive a load. The speed can be increased by decreasing the base doping, Q_B , decreasing base width, X_B , and increasing the average diffusion constant.

The magnitude of ratio of the collector current I_c to the emitter current I_E under active bias is defined as α_F . Then, the current gain β_F for the common emitter case is related to α_F by

$$\beta_F = \frac{\alpha_F}{1 - \alpha_F} \quad (2.24)$$

Typically, if the recombination of minority carriers in the base and the flow of holes into the emitter from the base are negligible, then the value of α_F will be close to unity and β_F will be very large.

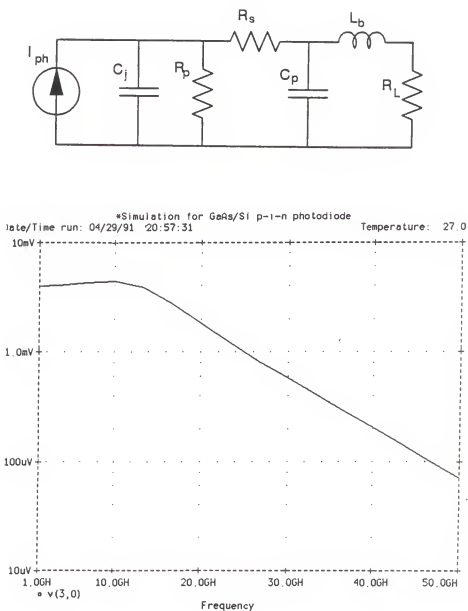


Figure 2.1 3-dB cutoff frequency simulation for the intrinsic and extrinsic RC equivalent circuit of a p-i-n photodiode.

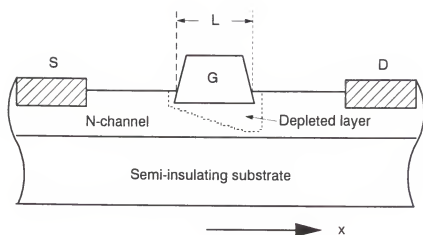


Figure 2.2 Schematic diagram of a MESFET.

CHAPTER 3

DEVELOPMENT OF DEVICES USING GaAs-ON-Si MATERIAL SYSTEM

3.1 Introduction

In this chapter, we discuss a high-speed and high-sensitivity planar GaAs and $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$ heterostructure Schottky barrier photodiode grown on p-type silicon substrate by molecular beam epitaxy (MBE). Growth of a thermally strained superlattice (TSL) buffer layer enables the fabrication of high performance GaAs Schottky photodiode on the silicon substrate. A reverse leakage current as low as 9×10^{-10} A for the device was achieved. The responsivity and quantum efficiency measured at 0.84 μm wavelength were found equal to 0.25 A/W and 37.5%, respectively. The response speed of this photodiode was measured by the impulse response method, which has a 70 ps risetime and a 3dB bandwidth of 5 GHz. In addition, a GaAs MESFET with a 1- μm gate length has also been successfully fabricated on the silicon substrate. The intrinsic transconductance of the device was around 140 mS/mm with f_T as high as 11 GHz. A simple hybrid integration of the photodiode with this MESFET yielded an output signal with full-width half maximum (FWHM) of 380 ps.

3.2 GaAs Schottky Barrier Photodetector on Si Substrate

The possibility of integrating high-performance GaAs photodetector with silicon circuits will allow interchip signals to be transmitted optically thereby eliminating or at least improving the fundamental limitations such as signal skew, maximum clock frequency and pin count and allowing more flexibility to the circuit designers. At the GaAs laser wavelength ($\sim 0.84 \mu\text{m}$), which is used as light source for interchip

communication, Si is absorptive ($\lambda_{gap}=1.06 \mu\text{m}$) and can be used directly as a detector medium without the need for GaAs-on-Si growth. However, GaAs does offer advantages, such as large absorption coefficient, high electron mobility, and large band gap energy, which make it a better material than silicon for high-speed optical detector application. In particular, a significant reduction in the absorption depth for incident light at GaAs laser wavelength (i.e. $\sim 10 \mu\text{m}$ for Si versus $\sim 1 \mu\text{m}$ for GaAs)⁶⁸ has a direct consequence in the potential gain-bandwidth product for GaAs photodiodes. Since gigahertz response usually requires carrier transit regions of only a few micrometers, a fast Si photodiode will be less sensitive than a similar GaAs photodiode, as well as being more vulnerable to the diffusion tail effects which can substantially degrade the frequency response. In this last regard, the possibility of band-gap tailoring with AlGaAs and the high mobility of GaAs which in turn increases the diffusion constant also favor GaAs detectors for reducing the diffusion tail effects. Furthermore, planar fabrication technology used in the development of Si integrated circuits is considered as one of the key advantages for the exploration of optoelectronic integration. Nevertheless, a minimum $10 \mu\text{m}$ absorption depth needed by Si is incompatible with the planar technology due to the out-of-focus problem occurred in the photolithography stage. On the other hand, the high absorption coefficient (hence, shallow absorption depth) of the GaAs offers significant guarantees its advantages for the planar fabrication technique.

3.2.1 Device Design

Previous works^{49,69} have shown that impulse response time of ~ 20 to 60 ps (FWHM) for a GaAs-on-Si photoconductive detector is attainable due to the short carrier lifetime. This is a result of high density of defects present in the GaAs layer, which in turn will reduce carrier lifetime and hence the detector response time. GaAs p-i-n photodiodes grown on Si substrates with a response time of 45 ps (FWHM) have been reported.⁴⁸ Avalanche photodiodes with a similar p-i-n structure have

also been investigated regarding dc operation with only a moderate gain (7x) being achieved because of large reverse leakage at high reverse bias.²⁶ Interdigitated metal-semiconductor-metal photodiode grown in a recess on Si with a response time of 80 ps (FWHM) has been reported.⁴⁷ All of the GaAs/Si photodiodes are suffering either from low photo-responsivity or large reverse leakage current which can be attributed to the existence of high dislocation density resulting from the large lattice mismatch and thermal expansion coefficient difference between GaAs and Si. Therefore further improvement in the development of GaAs photodetectors grown on Si substrates is highly desirable.

In this chapter, we present results of our study on a high performance, planar GaAs/Al_{0.3}Ga_{0.7}As Schottky barrier photodiode grown on silicon substrate by using the molecular beam epitaxy (MBE) technique. To reduce the dislocation propagation into the GaAs epi-layer, a TSL⁷⁰ layer was grown on Si-substrate during the GaAs growth. In addition to the dc characterization, we also performed the measurements of responsivity and response speed of the photodiode.

The main considerations in the design of a photodiode are the responsivity and the response speed. The responsivity, \mathfrak{R} , of a Schottky barrier photodiode can be obtained from Eq. 2.18 as

$$\mathfrak{R}(\lambda) = \frac{[T(\lambda)]\lambda}{1.24} \left\{ 1 - e^{\alpha w} \left(1 - \frac{\alpha L_{pn}}{\alpha^2 L_{pn}^2 - 1} \times \left[\alpha L_{pn} - \frac{\cosh(H'/L_{pn}) - e^{-\alpha H'}}{\sinh(H'/L_{pn})} \right] \right) \right\} \quad (3.1)$$

where

$T(\lambda)$ = the transmission coefficient of metal film

λ = the wavelength of the incident light

α = the absorption coefficient

w = the depletion layer width

H' = the thickness of the quasi-neutral base region.

The above expression is obtained by considering two main photo-currents coming

from the depletion region and the quasi-neutral base region. The response speed of a photodetector can be determined primarily by three parameters; the transit time, t_{tr} , across the depletion region, the diffusive time, t_{dif} , in the quasi-neutral region, and the RC time constant, t_{RC} , required to discharge the junction capacitance through a combination of internal and external resistances. The total risetime which is defined as the response time from 10 to 90% of a pulse height, is given by Eq. (2.15).

A high-speed Schottky barrier photodiode requires a small area and a large depletion layer width to ensure a low junction capacitance. However, increase the depletion width will in turn increase the carrier transit time which impedes the response speed. Therefore, the geometry and dimension of a photodiode as well as the doping density of the GaAs epi-layer should be optimized to achieve high-speed and high-sensitivity operation.

3.2.2 Thermal Supperlattice and Device Fabrication

The GaAs/Al_{0.3}Ga_{0.7}As planar Schottky barrier photodiode was grown on a p-Si substrate of (001) orientation tilted toward [110] direction according to the temperature profile shown in Fig. 3.1. After a pregrowth (975°C) heat treatment for oxide desorption, the substrate temperature was lowered to 480°C to initiate the buffer layer growth. The first growth stage involved deposition of a 900 Å (0.4 μm/h) GaAs layer, and the second step consisted of growth of a 3600 Å (1 μm/h) GaAs layer at 525°C. Following buffer layer growth, periodic thermal cycling (TSL growth) was carried out by ramping the substrate temperature up to 665°C and down to 400°C for 5 times (3600 Å each) without any growth interruption. Figure 3.2 shows the SEM cross-sectional view of the grown bufferlayer on top of the initial layer. Five periods of TSL can be seen by stain-etchant. Each thermal cycle took 4 minutes, and the second buffer growth resumed after the first thermal cycling growth. After completion of a 1.0 μm GaAs second buffer layer, a 0.3 μm of n-type GaAs doped to $1 \times 10^{18} \text{ cm}^{-3}$, a 0.1 μm of n-type Al_{0.3}Ga_{0.7}As, doped to $2 \times 10^{18} \text{ cm}^{-3}$, and a 0.8 μm undoped GaAs

were *insitu* grown subsequently on top of the buffer layer.

The detector structure used in this study is shown in Fig. 3.3. The planar geometry on the semi-insulating GaAs buffer grown on Si substrate can significantly reduce the parasitic capacitance. It is also shown the compatibility with the optoelectronic integration. To reduce the series resistance, a thin ($0.3\ \mu\text{m}$) heavily doped n^+ -GaAs layer is used for ohmic contact. In addition, to utilize the advantage of GaAs being able to do band-gap tailoring with AlGaAs, a $0.1\ \mu\text{m}$ $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$ n^+ -layer was deposited on top of the n^+ -GaAs layer. The undoped GaAs layer is used as the absorption layer. The illumination window was formed by a thin (100\AA) transparent Au film with a diameter of $20\ \mu\text{m}$. Using small active area can reduce the RC time constant, and thus improve the response speed of the photodiode.

3.2.3 Experiment and Results

To characterize the fundamental properties of the GaAs epilayer grown on Si, planar Schottky diodes with a $200\ \mu\text{m}$ diameter were fabricated. Some electrical properties of the Schottky diodes are summarized in Table 3.1. The lowest dark current obtained was $3\times 10^{-8}\text{A}$ at -5 V , and the best n -factor was around 1.2. Since the zero-bias depletion width is $0.64\ \mu\text{m}$, which corresponds to a junction capacitance of 6.2 pF , the diode requires only a very small reverse bias voltage to reach a fully depletion. The impurity level in the active undoped i -layer was estimated to be $7.5\times 10^{15}\text{ cm}^{-3}$ from the C-V measurements. The forward, reverse I-V and C-V curves of the Schottky diode are shown in Fig. 3.4, 3.5 and 3.6, respectively.

For the fabrication of photodetector, diode mesa was defined by photolithography and chemically etched by a solution of $\text{NH}_4\text{OH}:\text{H}_2\text{O}_2:\text{H}_2\text{O}$ (3:1:50) to about $0.9\ \mu\text{m}$ below the undoped active layer. The Schottky barrier and ohmic contact were formed by using a standard liftoff process. Au-Ge/Ni/Au ($400\text{\AA}:100\text{\AA}:600\text{\AA}$) alloy metal was used to form the ohmic contact by e-beam evaporation, and then annealed at 450°C for 120 sec in $\text{H}_2\text{-N}_2$ (5-95%) forming gas ambient to reduce the contact resistance.

A 100 Å Au film for the transparent Schottky barrier contact and a 600/1000 Å Ti/Au film for the bond pads were also formed by using e-beam evaporation after applying a plasma RF sputtered Si_3N_4 passivation. The thickness of the Si_3N_4 film was optimized by the quarter wave length design rule, and hence it is also used as antireflection coating film. To characterize the response speed of the fabricated photodiodes, test devices were mounted on a 50Ω microstrip transmission line made from a Cr-Au plated alumina substrate.

Current-voltage characteristic for the GaAs Schottky barrier photodiode grown on Si substrate is shown in Figure 3.7. Previously, large reverse leakage current was a common problem in GaAs-on-Si diodes, which has been attributed to defect assisted tunneling or conduction through metallic precipitates situated around dislocations.⁷¹ However, for the GaAs-on-Si photodiode reported here, the lowest leakage current obtained was 9×10^{-10} A (8×10^{-5} A/cm²) at -5 V bias, which is comparable to the conventional GaAs Schottky barrier diode fabricated on a GaAs substrate. This is attributed to the fact that TSL buffer layers used in our structure can reduce threading dislocations effectively.¹⁶ The improvement is believed to be the result of bending of dislocations by thermally induced stress. From previous study,⁷⁰ the x-ray linewidth of the observed rocking curve peaks from double-crystal x-ray diffraction has a large reduction from two to five thermal cycles. Additionally, buffer layer thickness before TSL growth also affects the effectiveness of TSL. A thin GaAs buffer near the interface contains a high density of twins and stacking faults, which tend to annihilate at ~ 4000 Å; too thick a buffer reduces the probability of dislocation coalescence. Typical dislocation density at the surface of a GaAs on Si film prepared with the insertion of five-period TSL and a proper initial buffer layer is 5×10^6 cm⁻². This low dislocation density is consistent with the result of low reverse leakage current of the photodiode reported here.

In addition to the low leakage current. The device also shows good photosensitiv-

ity. Figure 3.8 shows the measured external quantum efficiency and the responsivity of the GaAs Schottky barrier photodiode grown on Si substrate, which has a quantum efficiency of 28~42% and a responsivity of 0.11~0.25 A/W, respectively, for the wavelength range of 0.5~0.84 μm . This result is ten times better than those reported previously.⁴⁷ The improvement of responsivity in our photodiode is attributed to the reduction of bulk deep level trapping centers in the active region and effective control of the surface recombination by Si_3N_4 dielectric film passivation.

To measure the high frequency response of the detector, light pulse ($\lambda = 0.53 \mu\text{m}$) with a half width less than 30 ps and a repetition rate of 30 Hz were provided by frequency doubling of a 1.06 μm mode-locked Nd:YAG laser. The detected signal from the device mounted on a microstrip, was coupled via a delay line (5 GHz bandwidth) into a Tektronix S-26 sampling head ($t_r = 25$ ps) in a Tektronix 11802 digital sampling oscilloscope (See the insert in Figure 3.9). Figure 3.9 shows the output waveform of the detected signal from the sampling when the device was biased at 2 V. A risetime of 70 ps and a pulse width of 180 ps(FWHM) was obtained from the measurement. The impulse response was found to be limited by the bandwidth of the delay line unit. In our design, the device response speed is RC time constant limited. From C-V measurements, the capacitance of the photodiode was found to be 150 fF at -2V bias. Since the device series resistance is about 120 Ω , the RC time constant of 18 ps corresponds to a 3 dB cutoff frequency of 20 GHz.

3.3 GaAs MESFET on Si Substrate

3.3.1 Metal Contact

Control of the ohmic contact on III-V semiconductors is the key parameter to obtain a high performance field effect transistor. The most commonly used metallization system for III-V semiconductors is an eutectic mixture of Au/Ge (88%/12%)-x system, where x could be Ag, Ni or In. When heated above the eutectic temperature, the metal film melts and begins to etch the semiconductor. Alloying is initiated at

the portion where the melting starts, then it spreads to the whole contact area to form an alloy. Upon cooling, the semiconductor recrystallizes on the host lattice and freezes the dopants and the defects.

Alloyed ohmic contact can be characterized by the Transfer Length Method (TLM).⁷² The validity of this method is based on three conditions: (1) the current lines are normal to the metal-semiconductor interface, (2) the thickness of the metal and diffusion layers can be neglected, and (3) the current-voltage characteristic of the contact is linear. A typical three-terminal resistor structure is shown in Figure 3.10(a). It consists of three identical contacts to the semiconductor bar placed at distance ℓ_1 and ℓ_2 , while $\ell_1 \neq \ell_2$. The basic assumptions are that the difference between the width of the contacts W_c and bar W is negligible and that the contact resistance R_c for all three contact pads is equal. Then the following expression can be written for the total resistance R_1 and R_2 which correspond to the contact separations ℓ_1 and ℓ_2 :

$$R_1 = R_s(\ell_1/W) + 2R_c, R_2 = R_s(\ell_2/W) + 2R_c \quad (3.2)$$

where R_s is the sheet resistance of the line outside the contacts. Thus, R_c can be obtained by measuring the total resistance R_1 and R_2 . Solving for R_c , we obtain

$$R_c = \frac{R_2\ell_1 - R_1\ell_2}{2(\ell_1 - \ell_2)} \quad (3.3)$$

The disadvantage of the above expression is that the contact resistance is usually a small quantity and is thus extremely sensitive to the errors in measuring R_1 , R_2 , ℓ_1 and ℓ_2 . A better approach is to plot the total resistance as a function of the distance ℓ between several pairs of the planar contacts. Then, R_c is determined by linearly extrapolating to $\ell=0$ as shown in Figure 3.10(b).

3.3.2 MESFET Fabrication

For the MESFET fabrication, a mask set which contains 1- μm and 0.8- μm gate length devices, TLM patterns, and sidegate patterns was used. The GaAs MESFETs

were fabricated using standard GaAs processing techniques. Followed the mesa etching, Au-Ge/Ni/Au source-drain ohmic contacts were formed by evaporation/liftoff process and alloying at 450°C for 90 second in forming gas. Specific contact resistivity of $1 \times 10^{-6} \Omega \cdot \text{cm}^2$ was measured from TLM patterns on the same wafer. After recess etching of the n^+ -layer, aluminum gate was deposited. Shown in Fig. 3.11(a) is the top-view of two GaAs MESFETs on Si with $1 \times 50\text{-}\mu\text{m}$ gate and $3\text{-}\mu\text{m}$ source-drain spacing.

3.3.3 Integration of Photodiode with MESFET

Figure 3.12 shows the transistor characteristics of a typical depletion mode MESFET with a $1\text{-}\mu\text{m}$ gate length. The device pinches off well and shows good saturation characteristics. The transconductance vs. V_g curve taken at $V_{DS}=2.1 \text{ V}$ is shown in Fig. 3.13. Maximum transconductance is 110 mS/mm at $V_g=0.2 \text{ V}$. Taking into account the source-drain series resistance, typically $1 \Omega\text{-mm}$, the intrinsic transconductance is higher than 140 mS/mm. The influence of bias on the $I_D\text{-}V_{DS}$ characteristics of the neighboring devices is termed the sidegating effect. In this study, it has been measured with less than 15-percent decrease in drain current when a 5 V bias applied to a pad situated $5\text{-}\mu\text{m}$ away from the MESFET. The AC characteristics has also been measured by using an HP 8510 Network Analyzer between 100 MHz and 12 GHz. Figure 3.14 shows the current gain vs. frequency curve, a cutoff frequency of 11 GHz was estimated from this plot.

Figure 3.11(b) shows the top-view of a high performance MSM Schottky barrier photodiode fabricated on an undoped GaAs epitaxial layer ($0.8\text{-}\mu\text{m}$ thick) atop the n^+ FET channel layer. To reduce the series resistance, the highly doped ($3 \times 10^{17} \text{ cm}^{-3}$) n^+ FET channel is used for ohmic contact. Furthermore, to eliminate the long diffusion tail in the detector impulse response, a $0.1\text{-}\mu\text{m}$ n^+ $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$ -layer deposited on top of the n^+ -GaAs buffer layer. The $0.8\text{-}\mu\text{m}$ thick undoped n-GaAs layer used as the absorption layer. Active area of the photodiode is formed by a

thin (100\AA) transparent Au film with a diameter of $10\text{-}\mu\text{m}$. To reduce the noise of the photodiode, the reverse leakage current should be minimized. For the GaAs/Si photodiode reported here, the lowest reverse leakage current was found to be less than 9×10^{-10} A at -5 V. The maximum breakdown voltage obtained was larger than 20 V. The dark current and the photocurrent vs. reverse bias voltage under illumination by a $4\text{ }\mu\text{W}$ He-Ne laser light ($\lambda=6328\text{ }\text{\AA}$) are shown in Fig. 3.15.

Finally, a hybrid high-impedance front-end GaAs MSM detector/MESFET photoreceiver has been assembled using a $50\text{ }\Omega$ microstrip line. The impulse response of this photoreceiver module to a frequency-doubled YAG laser of 30 ps pulse width is shown in Fig. 3.16. The pulse width of the output signal (FWHM) is 380 ps, which suggests that the photoreceiver has a response speed of around 1 GHz.

3.4 Conclusion

In summary we have reported the development of a high performance GaAs Schottky barrier photodiode grown on Si substrate by MBE with the aid of the insertion of TSL as buffer layer. A low reverse leakage current of 9×10^{-10} A and a high responsivity of 0.25 A/W on this device have been achieved. This result brings the possibility for monolithic integration of the GaAs photonic devices with the Si integrated circuits directly on silicon substrates. A hybrid high impedance GaAs MSM photodiode and a MESFET integration on a $50\text{ }\Omega$ microstrip has shown about 1 GHz impulse response speed.

Table 3.1 Summary of the electrical properties of the GaAs Schottky diodes on Si substrate.

Summary of the Characteristics of
Mesa Diodes on R3383 Wafer

Diode #	Dark Current at -5V (Amp)	n-Factor	Barrier Height (eV)	Carrier Conc. at $w \approx 0.65 \mu m$	Capacitance (pF)
#(6,4)	3.3×10^{-8}	1.75	0.855	7.35×10^{15}	6.144
#(8,4)	4.0×10^{-8}	1.39	0.857	7.59×10^{15}	6.217
#(8,2)	9.2×10^{-7}	1.80	0.859	8.63×10^{15}	6.609
#(6,2)	6.7×10^{-7}	1.68	0.877	7.43×10^{15}	6.185

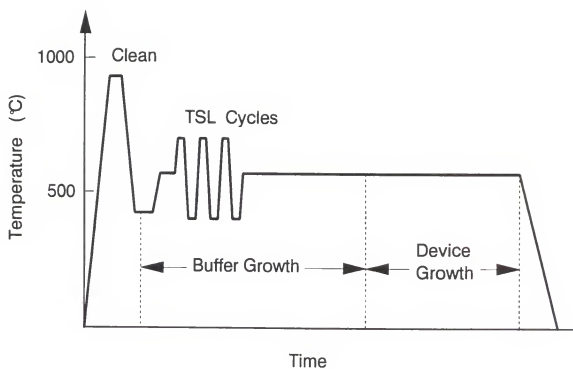


Figure 3.1 Growth temperature profile for the two-step GaAs grown on Si including thermal strained superlattice insertion.

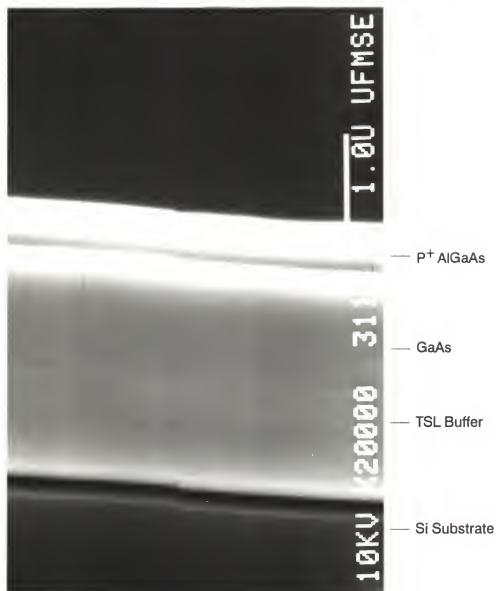


Figure 3.2 The SEM picture of MBE grown GaAs/Si layers revealed by stein-etching. The 5x TSL within the GaAs buffer layer is 3600 Å thick.

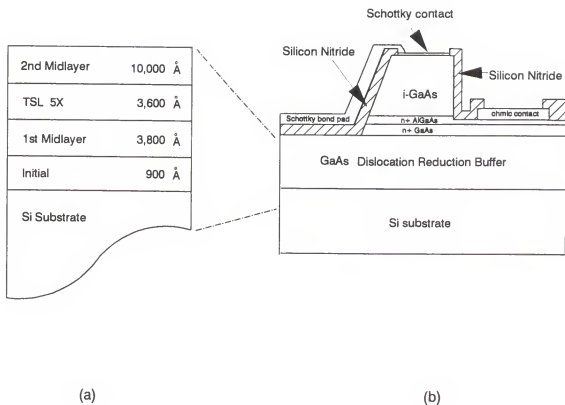


Figure 3.3 Schematic diagram of the planar GaAs/Al_{0.3}Ga_{0.7}As Schottky barrier photodiode grown on Si substrate. (a) A detailed view of the dislocation reduction GaAs buffer with the insertion of thermal strained superlattice. (b) A cross-sectional view of the device.

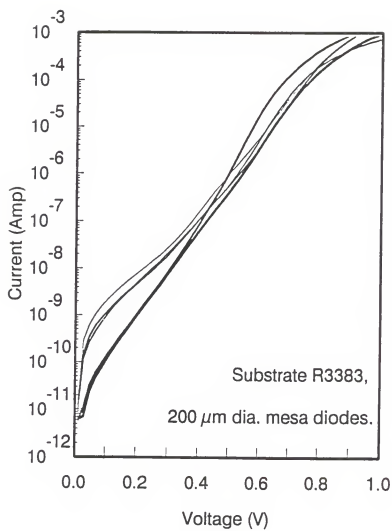


Figure 3.4 The typical forward current-voltage curves of the GaAs Schottky diodes on Si substrate.

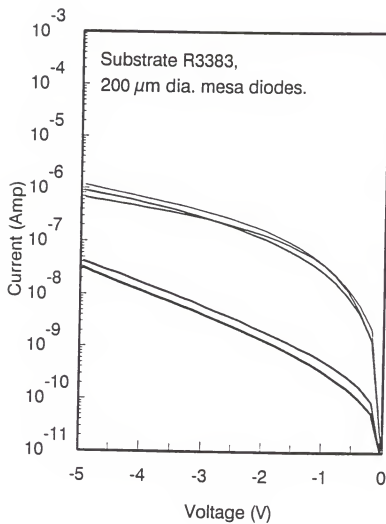


Figure 3.5 The typical reverse current-voltage curves of the GaAs Schottky diodes on Si substrate.

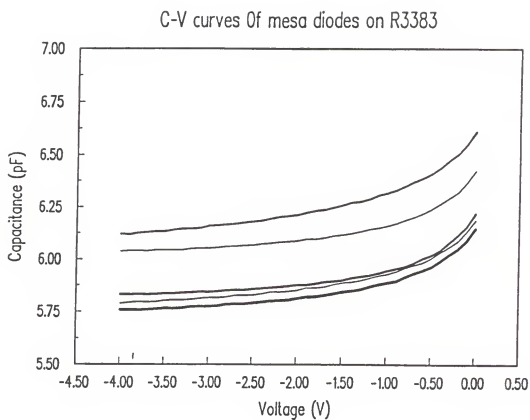


Figure 3.6 The typical 1 MHz capacitance-voltage characteristics of the GaAs Schottky diodes on Si substrate.

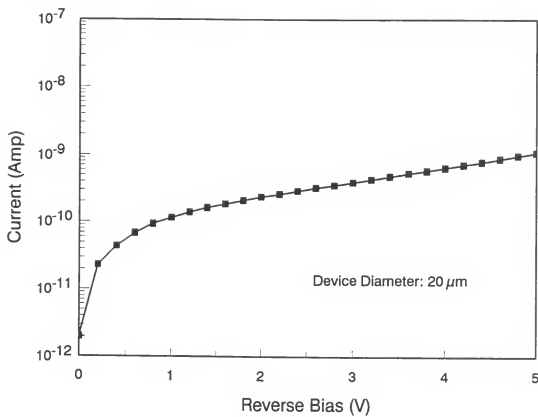


Figure 3.7 The reverse leakage current of a GaAs/ $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$ Schottky barrier photodiode grown on Si substrate.

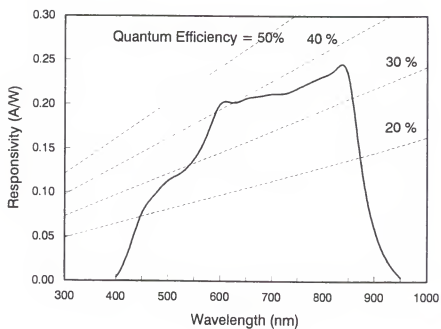


Figure 3.8 The spectral response of a GaAs/Al_{0.3}Ga_{0.7}As Schottky barrier photodiode grown on Si substrate. The active area of the photodiode is approximately $5.5 \times 10^{-6} \text{ cm}^2$.

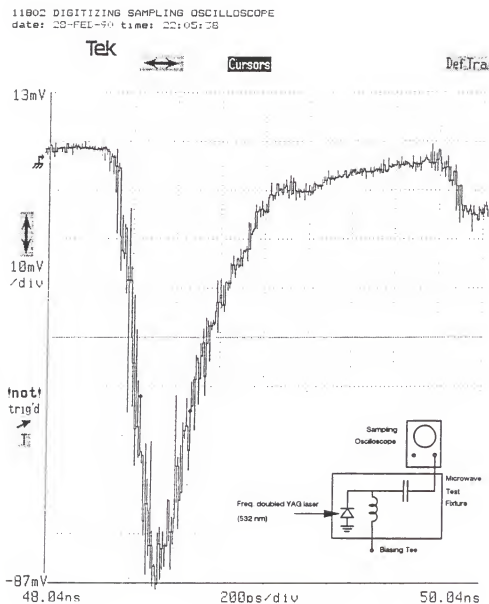


Figure 3.9 The response speed measurement of a GaAs/ $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$ Schottky barrier photodiode by the impulse response method. The insert shows the arrangement of the measuring apparatus.

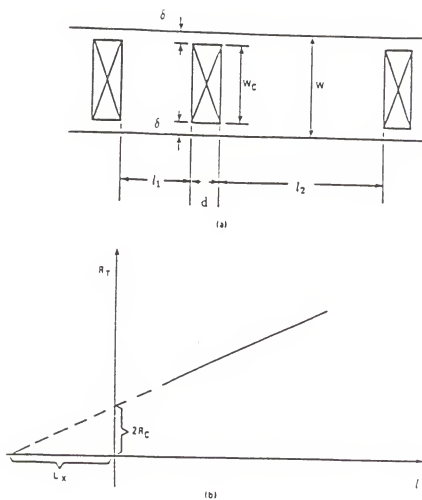


Figure 3.10 Implementation of the transfer length method (TLM) to the characterization of ohmic contact (a) pattern of the test structure (b) R_T versus length, ℓ , plot.

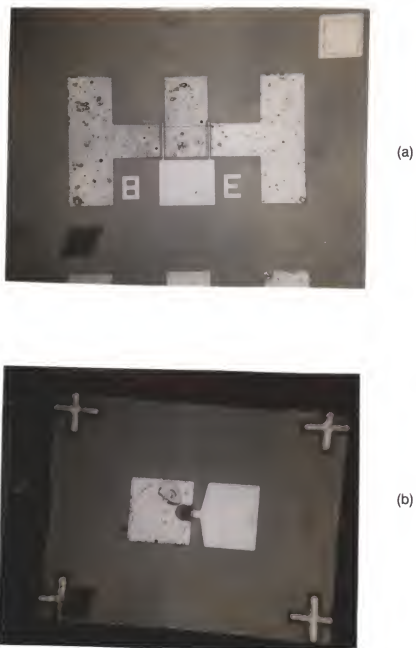


Figure 3.11 (a) Top view of a GaAs MESFET with a $1 \times 50\text{-}\mu\text{m}^2$ gate on Si substrate; (b) top view of a GaAs photodiode with $20\text{-}\mu\text{m}$ diameter on Si substrate.

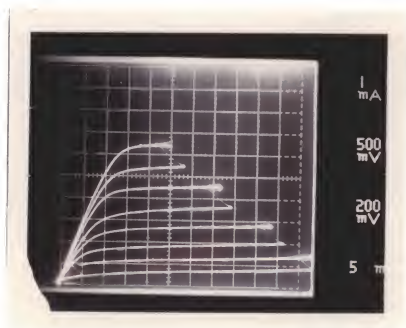


Figure 3.12 Transistor characteristics of a GaAs/Si MESFET with 1.0- μm gate. The top curve was obtained at $V_g=0$ and the V_g steps are 0.2 V.

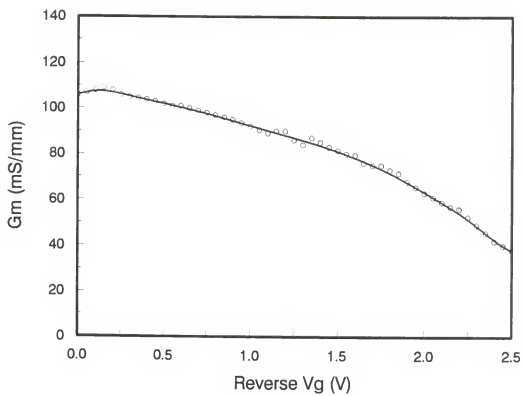


Figure 3.13 Transconductance of a GaAs/Si MESFET as a function of reverse gate-source voltage V_g .

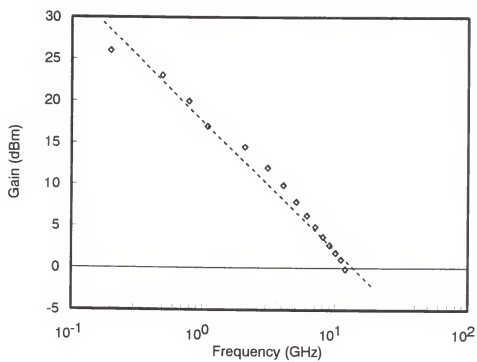


Figure 3.14 The current gain of a GaAs/Si MESFET as a function of frequency.

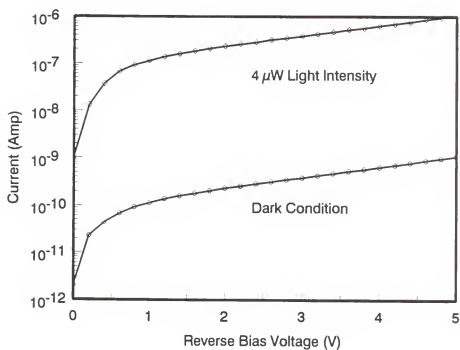


Figure 3.15 I-V characteristics of the GaAs MSM photodiode on Si substrate. The wavelength of the He-Ne laser source is 6328 Å.

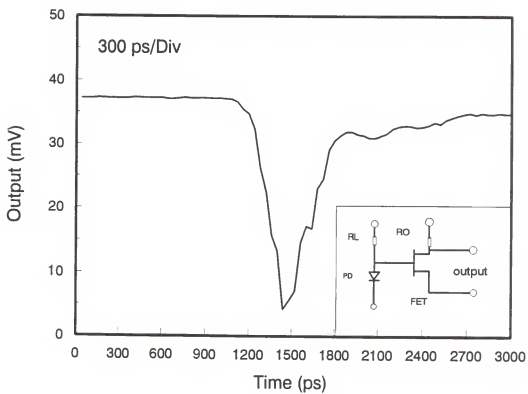


Figure 3.16 Impulse response of the photoreceiver to a frequency-doubled YAG laser with 30 ps pulse width (FWHM). The right-bottom corner shows the circuit diagram of the photoreceiver module.

CHAPTER 4

OPTIMIZATION OF GaAs/Al_{0.3}Ga_{0.7}As HIGH-SPEED SCHOTTKY BARRIER PHOTODIODE

4.1 Introduction

In the design of GaAs/Al_xGa_{1-x}As Schottky barrier photodiode, as we've discussed in Chap 3, the thickness of the device active layer has been reduced to accommodate the requirement of small transit time for high speed application. However, this reduction of thickness pays the price of sacrificing effective absorption depth for the wavelength of interest. For most III-V materials with absorption in the wavelength range of interest for fibre optical communication, i.e. 800 nm to 1600 nm, a thickness of approximately 2 μm is needed to absorb 88% of the light.⁶⁸ Based on the model of Bowers and Burras,⁷³ for a high-speed detector with $\alpha L \ll 1$, the quantum efficiency of a p-i-n photodiode is given by

$$\eta = (1 - R)\{1 - \exp(-\alpha L)\} \approx (1 - R)\alpha L \quad (4.1)$$

where α is the absorption coefficient, L is the thickness of the active layer, and R is the reflectivity of photodiode. Furthermore, in the transit-time-limit case, the bandwidth of the photodiode can be approximated as

$$f_{-3dB} = 0.45v/L \quad (4.2)$$

where v is the saturation velocity of the photogenerated carrier. Therefore, product of Eq. 4.1 and Eq. 4.2 gives

$$f_{-3dB} \cdot \eta = 0.45\alpha v(1 - R) \quad (4.3)$$

which is independent of geometric parameters. It implies no matter how we change the geometry of the photodiode, the bandwidth efficiency product will be a constant.

To enhance absorption in the active region of the photodetector, Chin and Chang⁷⁴ first proposed the resonance enhanced absorption by inserting multi-layer reflectors to a 475-nm thickness GaInAs photodiode. This technique has been applied to a number of photodetectors such as InGaAs phototransistors,⁷⁵ GaAs avalanche photodiodes,⁷⁶ and InP/InGaAs p-i-n photodiodes.⁷⁷ All of these detectors feature a very thin active layer to accommodate the quarter wavelength multiple requirement for resonance cavity. However, the natural characteristics of the resonance cavity reveal that if the incident photons are to be retained in the cavity, it means that the photons should not be easy to get out of the cavity. Nevertheless, photons which are not easy to go out of a cavity are also not easy to get in. This implies that how to couple the photons into the device is a challenge. On the other hand, the size of photodiode can not be reduced unlimited. The size of a typical single-mode fiber core (the smallest one) is about 25 μm . Any size of detector smaller than this will easily create the alignment problem. For a device with a 25 μm diameter, its junction capacitance with a 0.5 μm absorption thickness will be about 0.15 pf for the GaAs photodiode. Thus the RC time constant will be large enough to determine the speed of such a device. The advantage obtained by reducing the absorption layer thickness to reduce carrier transit time will become useless. Therefore, in this research, a reasonable thickness of 1 μm plus a multi-layer reflector inserted between the active region and substrate was proposed. This structure was designed to double the traveling length of the photons, while retains a reasonably low junction capacitance for the photodiode to assure a transit-time limited condition. In our design, resonance absorption was not considered. Thus, a scattering matrix (SC) technique⁷⁸ was used to design the GaAs/AlGaAs multi-layer reflector.

4.2 Optimization of Photodiode Design by a Scattering Matrix Technique

4.2.1 Scattering Matrix Technique

Considering the optical interface at $z=0$ as shown in Figure 4.1, $\phi_f(0^+)$ is the incident wave to the righthandside, $\phi_r(0^-)$ is the reflected wave to the lefthandside, $\phi_f(0^-)$ is the incident wave from the lefthandside, and $\phi_r(0^+)$ is the reflected wave from the righthandside. The relationship of these waves can be expressed by:

$$\text{reflected waves} = (\text{SC matrix})(\text{incident waves}) \quad (4.4)$$

or

$$\begin{bmatrix} \phi_f(0^+) \\ \phi_r(0^-) \end{bmatrix} = \begin{bmatrix} t & r' \\ r & t' \end{bmatrix} \begin{bmatrix} \phi_f(0^-) \\ \phi_r(0^+) \end{bmatrix} \quad (4.5)$$

where

t = transmission coefficient of EM wave travelling from left to right

r = reflection coefficient of EM waves travelling from left to right

t' = transmission coefficient of EM wave travelling from right to left

r' = reflection coefficient of EM wave travelling from right to left.

In Eq. (4.5), the matrix $\begin{bmatrix} t & r' \\ r & t' \end{bmatrix}$ is called the scattering (SC) matrix.

Now, considering another case shown in Figure 4.2, we have two sections divided by three points Z_1 , Z_2 , and Z_3 . These points represent the geometric points. There is no actual interface at these points, and hence there is no interface change of the wave function at each point. However, if we take the whole section as a piece, there are two components of waves coming into the section also two components of waves going out of the section. The relationship of these functions can also be expressed in a similar way as in Eq. (4.6), but with different SC matrices.

Therefore, for Z_1 - Z_2 section, we can write

$$\begin{bmatrix} \phi_f(Z_2) \\ \phi_r(Z_1) \end{bmatrix} = \begin{bmatrix} t_{21} & r'_{21} \\ r_{21} & t'_{21} \end{bmatrix} \begin{bmatrix} \phi_f(Z_1) \\ \phi_r(Z_2) \end{bmatrix} \quad (4.6)$$

For Z_2 - Z_3 section, the expression is given by

$$\begin{bmatrix} \phi_f(Z_3) \\ \phi_r(Z_2) \end{bmatrix} = \begin{bmatrix} t_{32} & r'_{32} \\ r_{32} & t'_{32} \end{bmatrix} \begin{bmatrix} \phi_f(Z_2) \\ \phi_r(Z_3) \end{bmatrix} \quad (4.7)$$

For the cascade of these two sections, we obtain

$$\begin{bmatrix} \phi_f(Z_3) \\ \phi_r(Z_1) \end{bmatrix} = \begin{bmatrix} t_{31} & r'_{31} \\ r_{31} & t'_{31} \end{bmatrix} \begin{bmatrix} \phi_f(Z_1) \\ \phi_r(Z_3) \end{bmatrix} \quad (4.8)$$

where

$$t_{31} = t_{32}(1 - r'_{21}r_{32})^{-1}t_{21}$$

$$r_{31} = r_{21} + t'_{21}r_{32}(1 - r'_{21}r_{32})^{-1}t_{21}$$

$$r'_{31} = r'_{32} + t_{32}(1 - r'_{21}r_{32})^{-1}r'_{21}t'_{32}$$

$$t'_{31} = t'_{21}(1 - r_{32}r'_{21})^{-1}t'_{32}.$$

4.2.2 Application of Scattering Matrix Technique to the Photodiode Design

Now, we can apply the SC matrix technique to the structure of a photodiode designed by Lee et al.⁷⁹ In a generalized form, we represent this GaAs/ $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$ Schottky photodiode as shown in Figure 4.3. Here we assume that the 100 Å Au-film is so thin that it is transparent to the incident light. The scattering matrix expressions for each interface and each section are given as follows:

For air-Si₃N₄ interface

$$\begin{bmatrix} \phi_f(0^+) \\ \phi_r(0^-) \end{bmatrix} = \begin{bmatrix} t_1 & r'_1 \\ r_1 & t'_1 \end{bmatrix} \begin{bmatrix} \phi_f(0^-) \\ \phi_r(0^+) \end{bmatrix} \quad (4.9)$$

For d₁-section

$$\begin{bmatrix} \phi_f(d_1^-) \\ \phi_r(0^+) \end{bmatrix} = \begin{bmatrix} e^{ik_1d_1} & 0 \\ 0 & e^{ik_1d_1} \end{bmatrix} \begin{bmatrix} \phi_f(0^+) \\ \phi_r(d_1^-) \end{bmatrix} \quad (4.10)$$

For the Si_3N_4 -GaAs interface:

$$\begin{bmatrix} \phi_f(d_1^+) \\ \phi_r(d_1^-) \end{bmatrix} = \begin{bmatrix} t_2 & r'_2 \\ r_2 & t'_2 \end{bmatrix} \begin{bmatrix} \phi_f(d_1^-) \\ \phi_r(d_1^+) \end{bmatrix} \quad (4.11)$$

For the d_2 -section:

$$\begin{bmatrix} \phi_f(d_2 + d_1^-) \\ \phi_r(d_1^+) \end{bmatrix} = \begin{bmatrix} e^{ik_2 d_2 - \alpha d_2} & 0 \\ 0 & e^{ik_2 d_2 - \alpha d_2} \end{bmatrix} \begin{bmatrix} \phi_f(d_1^+) \\ \phi_r(d_2 + d_1^-) \end{bmatrix} \quad (4.12)$$

For the GaAs-AlGaAs interface:

$$\begin{bmatrix} \phi_f(d_1 + d_2^+) \\ \phi_r(d_1 + d_2^-) \end{bmatrix} = \begin{bmatrix} t_3 & r'_3 \\ r_3 & t'_3 \end{bmatrix} \begin{bmatrix} \phi_f(d_1 + d_2^-) \\ \phi_r(d_1 + d_2^+) \end{bmatrix} \quad (4.13)$$

For the d_3 -section:

$$\begin{bmatrix} \phi_f(d_1 + d_2 + d_3^-) \\ \phi_r(d_1 + d_2^+) \end{bmatrix} = \begin{bmatrix} e^{ik_3 d_3} & 0 \\ 0 & e^{ik_3 d_3} \end{bmatrix} \begin{bmatrix} \phi_f(d_1 + d_2^+) \\ \phi_r(d_1 + d_2 + d_3^-) \end{bmatrix} \quad (4.14)$$

For simplicity, we have assumed in the above equations that the $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$ and the Si_3N_4 layers are transparent to the incident light. Thus, there is no absorption in those two layers.

Equations (4.9) through (4.14) can be cascaded as we have seen in the last section and can be solved iteratively by a numerical method. For an incident wavelength of $0.84 \mu\text{m}$, $d_1=1024\text{\AA}$, $d_2=0.9 \mu\text{m}$, $d_3=0.3 \mu\text{m}$, the total transmission through the device are calculated as 25.8%. From this calculation, it is obvious that a substantial amount of incident light is not absorbed by the device, which thus in turn reduces its quantum efficiency. Applying this technique to our GaAs/ $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$ /GaAs/Si device design, a transmission coefficient of 26% is obtained which is also large. To compensate this loss, we can add several $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$ and GaAs layers next to the n⁺-GaAs layer (see Fig. 4.4), then use the SC matrix method to optimize the thickness of d_5, d_7, \dots for a minimum of transmission through the device. For a six pair of $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$ /GaAs reflector design, the transmittance and reflection are calculated to be 17.2% and 0.59%, respectively.

4.3 Experiment and Results

To realize the device structure with the insertion of multi-layer reflector as shown in Fig. 4.4, the GaAs and AlGaAs reflector layer was grown by molecular beam epitaxy on the semi-insulating substrate. Fourteen periods of GaAs/Al_{0.3}Ga_{0.7}As reflector layers with GaAs layer thickness of 330 Å and Al_{0.3}Ga_{0.7}As layer thickness of 625 Å were grown on top of a 2000 Å GaAs buffer layer. This was followed by the growth of a 1000 Å AlGaAs layer and finally a 0.1 μm GaAs active layer. To ensure a low series resistance of the device, a 1000 Å AlGaAs and a multi-layer reflector were heavily doped to greater than $1 \times 10^{18} \text{ cm}^{-3}$. For the purpose of comparison, a control wafer without insertion of multi-layer reflector but with the same device structure was also prepared by the same MBE system in a separate run. The completed photodiode structure is that of a mesa with an annular top contact. This contact is designed to reduce the series resistance of the Schottky contact and simultaneously to facilitate top illumination. The fabrication was done by standard photolithography technique as mentioned in section 3.2.3. Au-Ge/Ni/Au(400Å:100Å:600Å) was used for the n⁺ ohmic contact.

Typical dark I-V characteristic curve of the multi-layer reflector photodiode is shown in Fig. 4.5 along with that of the control device. From the results, we see that the multi-layer reflector is electrical inactive and its presence does not degrade the quality of the GaAs active layer.

To characterize the responsivity of the photodiode at $\lambda=0.84\mu\text{m}$, a carefully designed optical experiment has been conducted. First, two device chips from multi-layer reflector and control wafer, were mounted on the same TO-5 package with 10 pins, with 3 test devices and 2 control devices wire-bonded on each package. The TO-5 package was then fastened on a KLINGER automatic x-y positioner with 0.5 μm resolution for each x or y increment. Right besides the TO-5 package, a well-calibrated reference detector from the United Detector Technology was mounted on

the same x-y positioner for the purpose of light source calibration. An Argon laser-pumped Ti-Sapphire laser was used as the light source. Its wavelength is tunable between 8000 to 9000 Å. In our experiment, the laser was tuned to 8400 Å. To obtain a good Gaussian beam, a 0.1 cm diameter orifice was used to define the beam size, then the beam was focused by a pair of microscope eye piece lens. The shape of the beam was determined by scanning the reference detector across the beam via an orifice of 10 μm diameter. The x- and y-direction scanned beam shape is shown in Fig. 4.6. After knowing the characteristics of incident light source, the responsivity of the test device or control device was obtained by measuring output photocurrent of the device under illumination. The results are 0.6 A/W, and 0.45 A/W for the test device and the control device at $\lambda=0.84\mu\text{m}$, respectively. This represents a 30% increase of responsivity compared with the control device without the multi-layer reflector. It also represents an 88% external quantum efficiency for the test device. This shows that besides some front surface reflection loss, the incident photons were absorbed effectively through the aid of the multi-layer reflector. The spectral response of the test device and control device between $\lambda=0.4$ to $0.9\mu\text{m}$ were also determined. They are shown in Fig. 4.7. The responsivity of the test device around $0.7\mu\text{m}$ wavelength was relatively low. It is believed to be due to the resonance absorption effect since the absorption depth for $\lambda=0.7\mu\text{m}$ is larger than $1\mu\text{m}$. To check the linearity of the test device to the input optical power, a photoresponse vs. input optical power curve at $\lambda=0.84\mu\text{m}$ was measured as is shown in Fig. 4.8. From this curve, it is seen that up to $60\mu\text{W}$, the device does not show any saturation effect.

4.4 Conclusion

We have successfully fabricated a GaAs Schottky photodiode with multi-layer reflector to increase the photo responsivity by 30% while retains both low transit time and small RC time constant. Photodiode with multi-layer reflector is possible to achieve both the high quantum efficiency and large bandwidth. In this chapter,

we have also demonstrated that the scattering matrix method can be used effectively to design the high performance photodiode with multi-layer reflector.

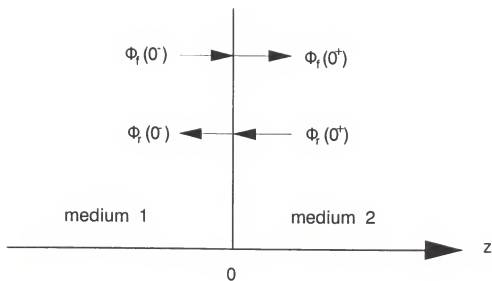


Figure 4.1 Changes of wave functions at the interface of two media. For simplicity, a 1-dimensional problem is assumed.

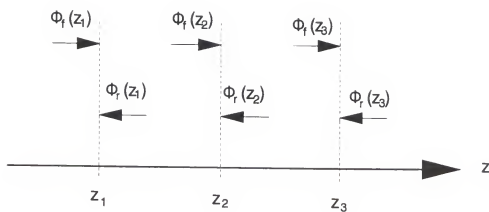


Figure 4.2 Schematics of the wave functions travelling through two imaginary sections of medium, Z_1 - Z_2 and Z_2 - Z_3 . Since the properties of the media are the same, there is no real optical interface.

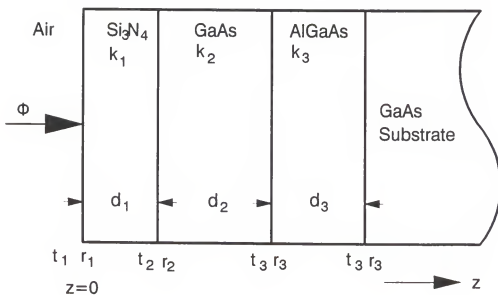


Figure 4.3 Simplified device structure of the GaAs/Al_{0.3}Ga_{0.7}As Schottky photodiode designed by Lee et al.⁷⁹ The reflectance back to the air and the transmittance into the semi-insulating substrate are calculated.

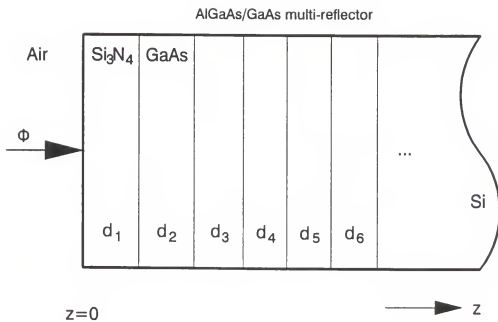


Figure 4.4 The novel $\text{GaAs}/\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$ Schottky photodiode structure with the additional $\text{GaAs}/\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$ multi-layer reflector grown on GaAs substrate.

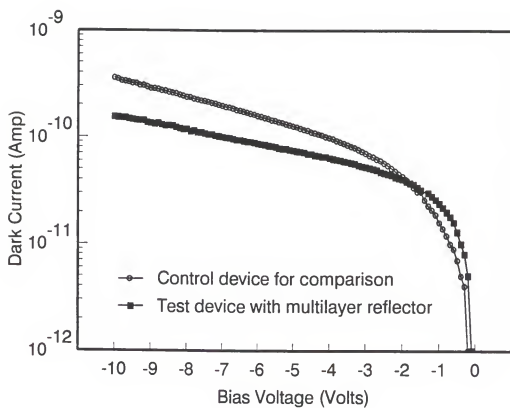


Figure 4.5 Typical dark I-V curves for the GaAs/AlGaAs photodiode with multilayer reflector for responsivity enhancement. The solid line is for the test device and the dot line is for the control device without the insertion of reflector.

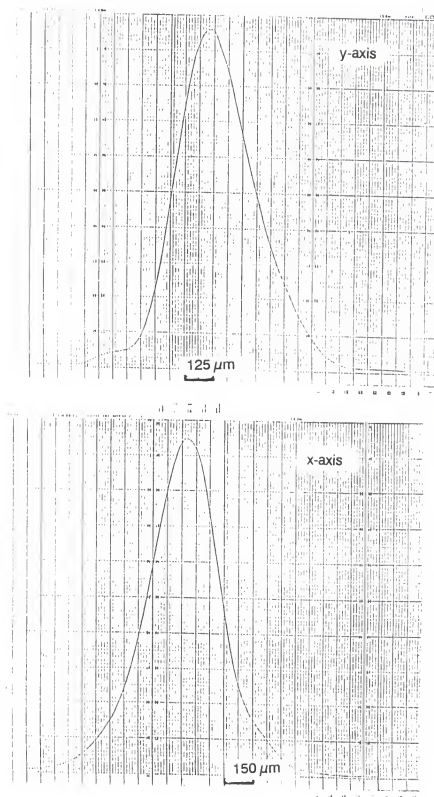


Figure 4.6 Beam shape of the incident Ti-sapphire tunable laser. Intensity of the beam was obtained by using a reference detector with 10 μm diameter orifice.

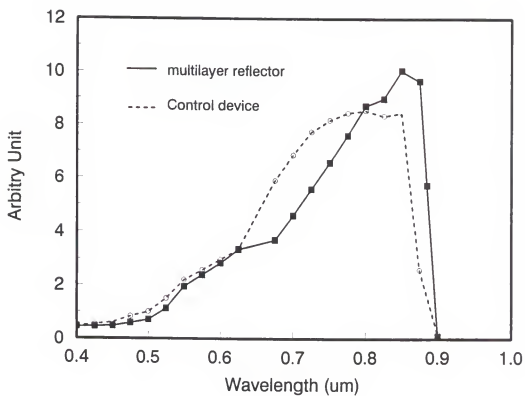


Figure 4.7 The responsivity spectrum of the GaAs/AlGaAs photodiode with multi-layer reflector between 0.4 to 0.9 μm wavelength. The solid line is for the test device and the dot line is for the control device without the reflector.

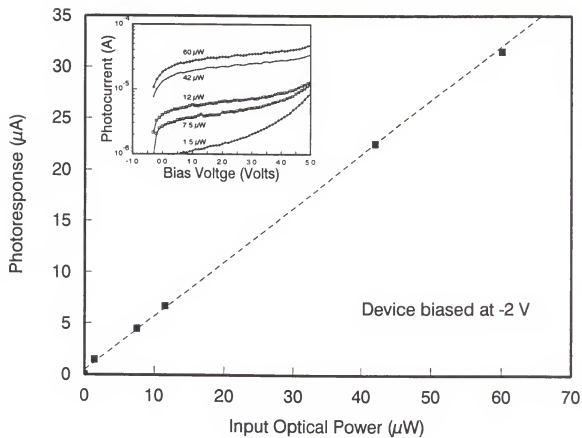


Figure 4.8 The photoresponse of the GaAs/AlGaAs photodiode with multi-layer reflector vs. input optical power.

CHAPTER 5

DESIGN AND ANALYSIS OF MULTI-GIGAHERTZ Si BJT PREAMPLIFIER

5.1 Introduction

The schematic diagram for a typical digital optical receiver for optical-fiber transmission system is shown in Fig. 5.1. The function of the receiver is to detect the incoming optical signal and to regenerate a stream of electrical signals for further processing. Therefore, the most important components in an optical receiver are the photodetector and the preamplifier. Together, these two elements determine many of the receiver characteristics as well as its performance. We have seen the results of GaAs Schottky barrier photodetector in the previous two chapters. In this chapter our efforts will be concentrated on the development of high-speed preamplifier. The preamplifier is difficult to realize due to the low-noise requirements as well as the single-ended operation.

Using the transistor to construct a preamplifier circuit, the noise figure of a GaAs FET is better than that of a Si BJT. However, several researchers^{1,80} have shown that for the transimpedance amplifier design, the noise performance of an FET-front-end is similar to the Si bipolar front-end design. For the reasons addressed in Section 1.1, Si BJT has been chosen for the design of preamplifier.

5.2 Design of Multi-Gigahertz BJT Preamplifier

In the design of a high-speed preamplifier, depending on the receiver configuration, there are two basic types as shown in Fig. 5.2, i.e., high impedance and transimpedance amplifier. The high-impedance amplifier^{17,81–83} offers a lower noise

level and hence a higher detection sensitivity. However, because of the high impedance at the front end, the frequency response is limited by the RC time constant at the input. Thus an equalizer following the amplifier is necessary to extend the receiver bandwidth up to the desirable value. This requirement introduces complexity into the receiver design where the pole of the amplifier response needs to be matched with the zero of the equalizing network. Since the amplifier pole is not a constant, a resulting pole-zero mismatch is likely to degrade the receiver performance. Furthermore, the high-impedance design has another drawback of limited dynamic range. This is due to the high input load resistance.

The transimpedance amplifier design⁸⁴⁻⁸⁶ is a more common approach to avoid the dynamic range problem. In addition, it is normally designed to take advantage of the negative feedback effect so that the amplifier bandwidth is extended to the desired value. Thus no equalization measure is required. Usually, the transimpedance receiver noise level is higher and the receiver sensitivity is less than that of a high-impedance design because of the thermal noise of the feedback resistor. However, in the multi-gigahertz region, there are some other noise factors, which we will discuss in detail later on, to dominate the receiver noise contribution. Thus, transimpedance amplifier is indeed a better choice for the high-speed application.

5.2.1 Amplifier for Capacitance Source

In the fiber-optic receiver, the signal source is a photodetector such as a p-i-n photodiode or a MSM photodiode. Presently, a MSM photodiode is more popular in the integrated photoreceiver circuit. The equivalent circuit of the signal source consists of a current source in parallel with a small capacitance as shown in Figure 5.3. The value of capacitance C_s can range from several pF in the case of packaged p-i-n photodiode with moderate bias to less than 0.1 pF in the case of monolithic integrated MSM photodiode. In this work, we choose on-chip or monolithic design. Therefore, a range of 0.1 pF to 1 pF of C_s has been used in the design and analysis.

A number of discrete or monolithic circuit realizations for such a preamplifier have been published.⁸⁷⁻⁹⁰ In this thesis an effective preamplifier circuit for use in these applications is described. The basic circuit schematic is shown in Fig. 5.4 with element values for a design with 3-dB bandwidth of approximately 2 to 7 GHz. A shunt-series feedback over three stages is used to allow the use of a larger value of R_F giving a minimum noise contribution. The actual noise figure will be discussed in next section. The transresistance from i_s to the emitter of Q_3 is approximately R_F . The value of I_{C1} should be as low as possible in order to minimize the noise current contribution of I_{B1} . The emitter follower Q_2 is added to the basic feedback pair to maximize the loop gain and reduce capacitive loading at the high impedance collector of Q_1 .

In practice, first we consider the frequency response of circuit. Since Q_2 and Q_3 are wide-band emitter followers, the forward-path frequency response can be characterized by the small-signal equivalent circuit of Q_1 shown in Fig. 5.5, where

$$R_a = r_{\pi 1} // r_{b1} // R_F \quad (5.1)$$

$$C_a = C_s + C_{\pi 1} \quad (5.2)$$

$$R_b = R_l \quad (5.3)$$

$$C_b = C_{cs1} + C_{\mu 2} \quad (5.4)$$

In the above equations, $r_{\pi 1}$, r_{b1} , $C_{\pi 1}$, and C_{cs1} are the parameters of the small-signal equivalent circuit of Q_1 , and $C_{\mu 2}$ is the collector-base capacitance of Q_2 .

To solve the circuit in Figure 5.5, summation of currents at B gives

$$i_1 = \frac{v_1}{R_a} + v_1 C_a s + (v_1 - v_2) C_{\mu} s \quad (5.5)$$

Summation of currents at C gives

$$g_{m1} v_1 + \frac{v_2}{R_b} + v_2 C_b s + (v_2 - v_1) C_{\mu} s = 0 \quad (5.6)$$

Eq. (5-6) can be written as

$$v_1(g_{m1} - C_\mu s) = -v_2\left[\frac{1}{R_b} + (C_b + C_{\mu 1})s\right] \quad (5.7)$$

Thus

$$v_1 = -v_2 \frac{\frac{1}{R_b} + (C_b + C_\mu)s}{g_{m1} - C_\mu s} \quad (5.8)$$

Substituting Eq. (5-8) into Eq. (5-5) gives

$$\begin{aligned} i_1 = & -v_2\{1 + [C_a R_a + C_b R_b + C_{\mu 1}(R_a + R_b + R_a R_b g_{m1})]s \\ & + [C_a C_b + C_{\mu 1}(C_a + C_b)]R_a R_b s^2\} / R_a R_b (g_{m1} - C_\mu s) \end{aligned} \quad (5.9)$$

so the transfer function of the circuit can be calculated as

$$\frac{v_2}{i_1} = -\frac{R_a R_b g_{m1} (1 - \frac{C_{\mu 1}}{g_{m1}} s)}{D(s)} \quad (5.10)$$

where the denominator $D(s) \simeq 1 - \frac{s}{p_1} + \frac{s^2}{p_1 p_2}$ (Here we assume $p_2 \gg p_1$)

Therefore, the dominant pole is

$$p_1 = \frac{1}{(C_a + C_{\mu 1})R_a + (C_b + C_{\mu 1})R_b + C_{\mu 1}R_a R_b g_{m1}} \quad (5.11)$$

The second pole is

$$p_2 \cong -\frac{g_{m1} C_{\mu 1}}{C_a C_b + C_{\mu 1}(C_a + C_b)} \quad (5.12)$$

The dominant pole p_1 is determined by the equivalent parallel $R_i - C_i$ circuit seen at the input by the current source i_s . The input resistance R_i is dominated by resistive Miller effect due to R_F . However, because the very small C-B capacitance (only 3.9 fF) of the sub-micrometer BJT used in this design, the Miller capacitance in Q_1 is not dominant. Therefore Eq. (5.11) can be reduced to

$$|p_1| \cong \frac{1}{R_F(C_s + C_{\mu 1} + g_{m1} R_1 C_{\mu 1})} = \frac{1}{R_F[C_s + (1 + g_{m1} R_1)C_{\mu 1}]} \quad (5.13)$$

Since $g_{m1} = \frac{d}{dV_{BE}}(I_s \exp \frac{V_{BE}}{V_T}) = \frac{I_{s1}}{V_T}$, Eq. (5-13) can be written as

$$|p_1| = \frac{1}{R_5 C_i} \quad (5.14)$$

where $C_i = C_s + (1 + \frac{V_1}{V_T})C_{\mu 1}$, $V_1 = I_{c1}R_1$ is the dc voltage drop across R_1 , and $V_T = kT/q$.

From Eq. (5.14), we can estimate the amplifier -3dB frequency as

$$f_{-3dB} = \frac{A}{2\pi R_5 C_i} \quad (5.15)$$

where A is the close loop gain of the preamplifier.

On the other hand, Eq. (5.12) shows that as g_{m1} is reduced, which in turn implies that I_{c1} is reduced, $|p_2|$ is reduced and eventually will cause unacceptable phase margin in the loop. For the process technology used, $C_{\mu 1} = 3.9$ fF, $C_b = 16.1$ fF, and several iterations gives a minimum acceptable value of $I_{c1} = 0.64$ mA with acceptable phase margin. Note that for noise consideration, I_{c1} should be as small as possible and the lower limit is set by the second most dominant pole of the feedback loop. For a photodiode with 0.5 pF capacitance and $C_{\mu 1} = 3.9$ fF, $A = 10$ and a reasonable estimation of $R_F = 2.1$ K Ω to ensure a low noise figure, to achieve a 3-dB frequency response of 4 GHz, R_1 is chosen to be 4.5 K Ω .

Other resistor values of the circuit are chosen as follows. A nominal bias current of 0.9 mA in Q_2 is set by $R_2 = 2$ K Ω . For the output stage bias design, it is convenient to set $R_3 = R_4$ since this gives one V_{BE} drop across R_3 . Values of $R_3 = R_4 = 160$ Ω give $I_{c3} = 3.5$ mA and a parasitic pole well above ten gigahertz range.

5.2.2 Noise Estimation

When the front-end active device of a transimpedance amplifier is a bipolar junction transistor, the input equivalent noise current power is given by^{25,91}

$$\overline{i_{na}^2} = \frac{4KT}{R_F} I_2 B + 2qT_{B1} I_2 B + \frac{2qI_{c1}}{g_{m1}^2} [2\pi(C_s + C_{\mu 1})]^2 I_3 B^3 + 4KT r_{b1} (2\pi C_s)^2 I_3 B^3 \quad (5.16)$$

Where B is the bandwidth of preamplifier, r_{b1} is the base resistance of transistor, and I_2 and I_3 are definite integrals which depend on the pulse shape of input signal. For a rectangular shape input signal with well-defined shape and clean pulse edge. $I_2 \simeq$

0.5, and $I_3 \simeq 0.04$.²⁵ Therefore Eq. 5.16 can be written as

$$\overline{i_{na}^2} \cong \left(\frac{2KT}{R_F} + qI_{B1} \right) B + \frac{3qI_{c1}}{g_{m1}^2} (C_s + C_{\mu 1})^2 B^3 + 6KT r_{b1} C_s^2 B^3 \quad (5.17)$$

Assuming $\beta_1 \approx 50$ and $C_s=0$ Eq. 5.17 gives $i_{na}=20$ nA rms in a 4GHz bandwidth. Since capacitance of photodiode can not be zero, for $C_s=1$ pf, and $r_{b1}=200 \Omega$, $i_{na}=75$ nA in 4 GHz bandwidth.

Conventional preamplifier argument shows that the relatively lower R_F value than that of the value in the high impedance design is the main reason of poor noise performance for transimpedance amplifier. But this is only true in the sub-gigahertz bandwidth design. From Eq. 5.17, it is clear that the frequency-dependent terms cause the rapid increase of noise as the bandwidth increases. If we further look into the components of the two frequency-dependent terms, only the first one can be optimized by fine tuning the values of I_{c1} and g_{m1} on circuit level. The rest depends on the quality of the transistor and photodiode used. Therefore, we can state that in the GHz region, the design criteria are more sensitive to the change of bandwidth. They are also more sensitive to the changes of the parameters of the active device used, i.e., the preamplifier performance is more dependent on device performance.

5.3 Simulation and Analysis

The preamplifier circuit designed in section 5.2 was then simulated by using ASTAP circuit simulator. To perform the simulation, a Si BJT device model of a sub-micrometer self-aligned bipolar technology⁹² has been used. Description of the technology and results of the simulation are given as the follows.

5.3.1 High Performance Bipolar Technology

To achieve the gigahertz bandwidth performance, it demands a high-speed bipolar transistor technology. Recently, the most common advanced bipolar technologies

are based on self-aligning double-polysilicon processes. By applying polysilicon base and emitter contacts which are self-aligned against each other, a drastic shrinking of the parasitic part of the transistor can be achieved. As a consequence of this lateral shrinkage, the base spreading resistance and the collector junction capacitance are considerably reduced. Several well-proven modifications of the basic double-poly technology have been developed which allow a further increase in operating speed and packing density.⁹³⁻⁹⁶

The cross section of the transistor used in this study is shown in Fig. 5.6. This technology features minimized device topography and shallow profiles in addition to the trench isolation to reduce the isolation capacitance and transistor size. Typical device parameters for a n-p-n transistor with $A_E = 0.5 \times 4.0 \mu\text{m}^2$ is shown in Table 5.1. These parameters have been used in the design of the preamplifier circuit. The Gummel plot for the n-p-n transistor can be seen in Fig. 2 of Reference 92. Its maximum cutoff frequency f_T is 26.2 GHz.

5.3.2 Simulation and Analysis

The simulation of the preamplifier was performed by using ASTAP circuit simulator. ASTAP is a comprehensive industrial type circuit simulator developed at IBM T.J. Watson Research Center. The tool is installed on an IBM 3090 main frame machine under the MVS operating environment. It has the capability of including FORTRAN subroutines and functions in its source file.

The accuracy of the simulation depends on the accuracy of the transistor device model. Corresponding to the sub-micrometer technology used in the circuit design, the device model used in the simulation is shown in Fig. 5.7. The values of the parameters are obtained from actual measurement of the discrete devices fabricated in the same process. The model and its parameter values have been fine tuned to obtain a $\pm 20\%$ accuracy between the circuit simulated and actually fabricated.

By changing the value of the capacitance of the photodiode C_s from 0.1 to 1.0

pF, a set of Gain (closed loop)-frequency curves were obtained for the preamplifier designed in Section 5-2 (See Fig. 5.8). In the figure IRC.Q03, L/1, IRC.Q03, L/2, IRC.Q03, L/3, and IRC.Q03, L/4 represent the curves for $C_s=0.1, 0.2, 0.5$ and 1.0 pF, respectively. The corresponding -3dB bandwidths for the four cases are 7, 5.4, 3.6 and 2.5 GHz, respectively. In the design of the preamplifier, we have used $C_s=0.5$ pF to obtain a bandwidth of 4 GHz. Both results are in good agreement. The corresponding phase-frequency curves are shown in Fig. 5.9. At the -3dB bandwidth the phase margins are $25^\circ, 30^\circ, 35^\circ$, and 42° for $C_s=0.2, 0.2, 0.5$ and 1.0 pF, respectively. The phase margin for the 0.1 pF case is relatively small. Since the shape of the pulse response in this case doesn't show a serious overshoot, it is still acceptable. The rest phase margins are reasonably good enough to maintain a stable operation of preamplifier at such high frequency. To check the validity of the design further, the open-loop and feedback loop equivalent circuits were constructed. Then, simulations under the same DC operating condition were performed. The gain-frequency curves of the results are shown in Fig. 5.10. At low frequency region open-loop gain is 52 dB and feedback loop gain is 33 dB. If we recall the low-frequency closed-loop preamplifier gain of 19 dB, it is shown that these values are fitted perfect to the well know feedback amplifier gain equation⁹⁷

$$A = \frac{a_o}{1 + T_o} \quad (5.18)$$

where A is the overall amplifier gain, a_o is the open loop amplifier gain and T_o is the feedback loop gain. In addition, the shift of the -6dB/octave corner frequency from the low frequency in open-loop case to the high frequency in closed-loop case also confirms the that dominant pole frequency $|p_1|$ has improved to the value of $(1+T_o)|p_1|$ as clearly shown in Fig. 5.10. To investigate the dynamic range of the preamplifier, a time domain simulation with an input current signal of rectangular wave shape has been performed. The amplitudes of the input current signal were varied from 0.1 to 1 mA. the results is shown in Fig. 5.11. In the figure JSTRT/1R is the waveform of the

input current signal. Its amplitude was varied from 0.1, 0.2, 0.5 to 1.0 mA peak and its period is 0.5 ns. Shown here is only the case of 1.0 mA peak. NC3/1L, NC3/2L, NC3/3L, and NC3/4L are the outputs of the preamplifier corresponding to the input current signal of 0.1, 0.2, 0.5, and 1.0 mA peak, respectively. It is obvious that the output voltage wave shape does not saturate up to 0.5 mA peak current. Hence a dynamic range of 45 dB has been obtained for this preamplifier circuit design.

5.4 Conclusion

In this chapter we have presented the design, simulation, and analysis of a multi-gigahertz preamplifier by using the state of art double-poly self-aligned Si bipolar IC technology. As high as 7 GHz preamplifier design has been achieved. Which corresponds to a non-return-to-zero digital signal of greater than 10 gigabit per second. Since the simulation and layout of this design were done by the standard state of art industrial process. The simulated results can be expected to be very close to the actual circuit implementation.

Recently, Schichijo et al.⁹⁸ have demonstrated a monolithic process to co-integrate Si CMOS and GaAs MESFET devices and circuits on a silicon chip through epitaxial growth of a GaAs layer on a prefabricated Si wafer. Because of this breakthrough, it is feasible to realized the co-integration of high speed GaAs photodetector presented in Chapter 3 with the multi-gigahertz Si BJT preamplifier described in this chapter.

Table 5.1 Typical device parameters for the double-poly self-aligned bipolar transistor.

Emitter Area	A_E	$0.5 \times 4.0 \text{ } \mu\text{m}^2$
Current Gain	H_{FE}	50
E-B Breakdown	BV_{EBO}	4.5 V
C-B Breakdown	BV_{CBO}	25.0 V
E-C Breakdown	BV_{CEO}	5.1 V
E-B Capacitance	C_π	6.6 fF
C-B Capacitance	C_μ	3.9 fF
C-S Capacitance	C_{CS}	12.2 fF
Base Resistance	R_B	164 Ω
Emitter Resistance	R_E	14.0 Ω
Cutoff Frequency	f_T	26.2 GHz

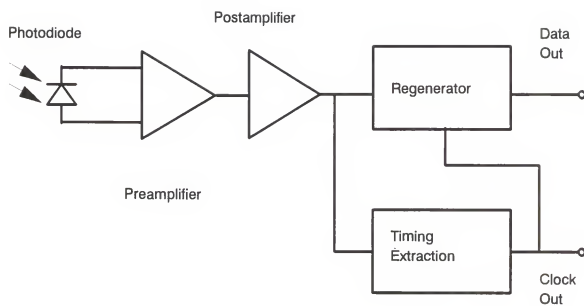
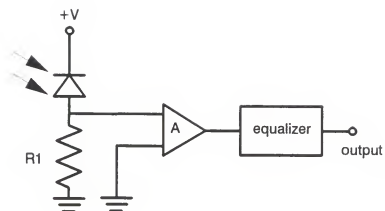
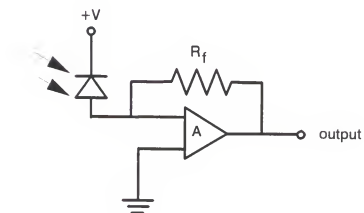


Figure 5.1 Scheme diagram of a typical digital optical receiver.



(a)



(b)

Figure 5.2 Typical optical receiver amplifier design (a) high impedance (b) transimpedance.

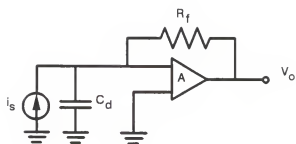


Figure 5.3 Equivalent circuit of a typical transimpedance amplifier with driving source.

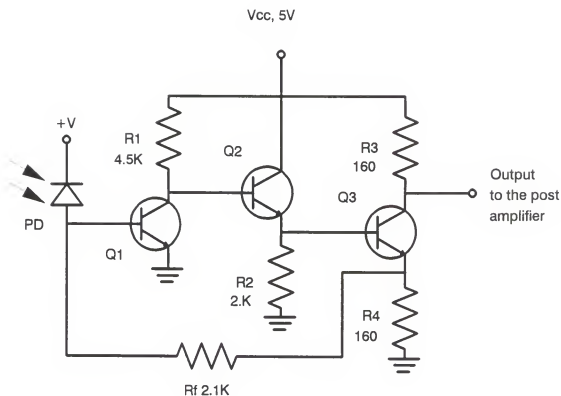


Figure 5.4 Basic schematics of a high speed BJT transimpedance amplifier design.

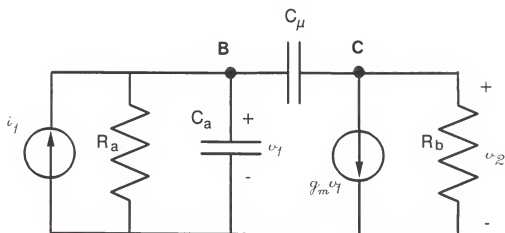


Figure 5.5 Small-signal equivalent circuit of Q1 as a common-emitter amplifier using a Norton equivalent circuit at the input.

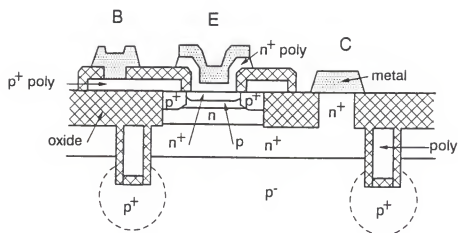


Figure 5.6 Schematic cross section of the double-poly self-aligned bipolar transistor.

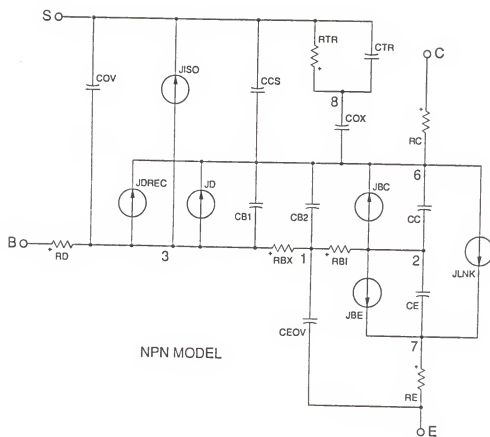


Figure 5.7 The equivalent circuit model of the n-p-n transistor used in the simulation of high speed preamplifier.

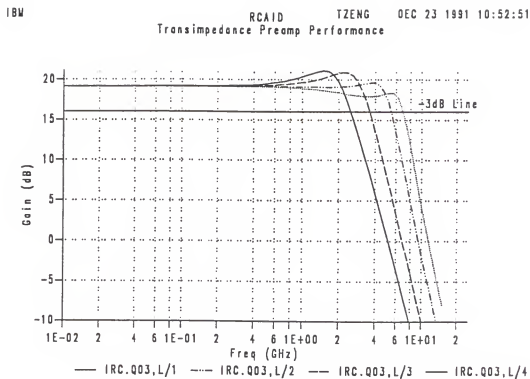


Figure 5.8 Closed-loop gain vs. frequency curves of the preamplifier. In the figure IRCQ₃, L/1, L/2, L/3 and L/4 are the curves for photodiode capacitance $C_s=0.1, 0.2, 0.5$ and 1.0 pF, respectively.

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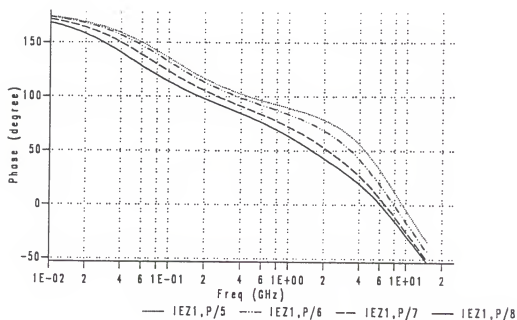


Figure 5.9 Phase margin vs frequency of the preamplifier shown in Figure 5.4. In the figure IEZ1, P/5, P/6, P/7 and P/8 are the curves for $C_s=0.1, 0.2, 0.5$, and 1.0 pF, respectively.

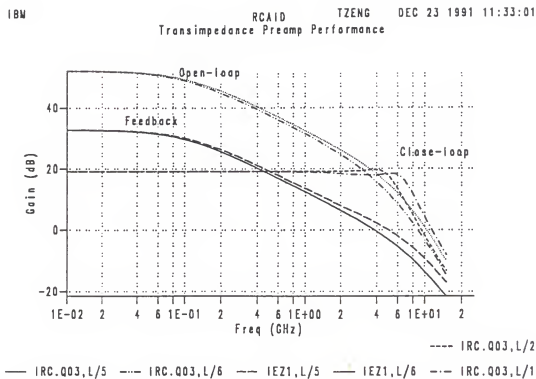


Figure 5.10 Shift of the dominant pole corner frequency and the effect of feedback loop to the change of circuit gain. Figure shown is the results for $C_s=0.1$, and 0.2 pF, respectively.

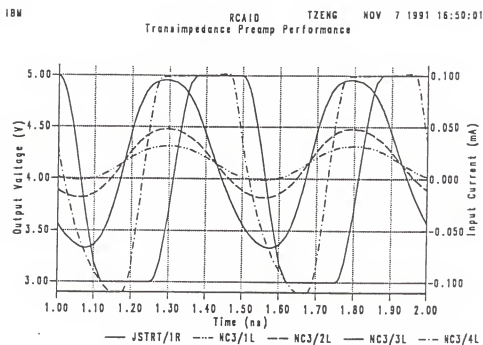


Figure 5.11 The time-domain response of the amplifier circuit to a rectangular current signal. In the figure, JSTRT/1R is the input current signal for $I_{pk}=1.0$ mA, curves of NC3/1L, NC3/2L, NC3/3L, and NC3/4L are the output voltages for $I_{pk}=0.1, 0.2, 0.5$, and 1.0 mA, respectively.

CHAPTER 6

DEVELOPMENT OF PHOTODIODE USING $\text{In}_{0.4}\text{Ga}_{0.6}\text{As}/\text{GaAs}$ MATERIAL SYSTEM

6.1 Introduction

In this chapter, we described the successful development of a planar, low dark current, and high sensitivity $\text{In}_{0.4}\text{Ga}_{0.6}\text{As}$ p-i-n photodiode fabricated on a semi-insulating GaAs substrate with the aid of a multistage strain-relief buffer system. Without using surface passivation and antireflection coatings, the detector has a quantum efficiency of 42 % and a peak responsivity of 0.45 A/W at 1.3 μm wavelength. The reverse leakage current for the mesa-etched photodiode with an active area of $2 \times 10^{-4} \text{ cm}^2$ is $5 \times 10^{-9} \text{ A}$ at - 5 V, and the breakdown voltage exceeds 25 V.

To further study the quality of the p-i-n photodiode prepared on the lattice mismatched $\text{In}_{0.4}\text{Ga}_{0.6}\text{As}/\text{GaAs}$ material system, the generation lifetime profile in the i-region of the photodiode has been determined by using a differential current-voltage (I-V) and Capacitance-Voltage (C-V) technique. In addition, the generation lifetime and deep-level defects in these p-i-n photodiodes were also determined by the deep-level transient spectroscopic (DLTS) measurements. A single-level electron trap has been detected by the DLTS measurement. Energy level, trap density, and the capture cross-section of the trap was also determined. Relatively high generation lifetime of 10^{-8} second was obtained which is consistent with the low dark current obtained in our device.

6.2 Device Quality InGaAs Layer Grown on GaAs

High-speed and large bandwidth p-i-n photodiodes are important components for optical communication systems operating in excess of 1-2 Gbit/s, particularly,

for systems using heterodyne detection where the detector bandwidth must be more than twice the bit rate. For long distance fiber optical communication systems, the minimum attenuation loss in existing silica fibers occurs at $1.55\text{ }\mu\text{m}$, while $1.3\text{ }\mu\text{m}$ represents a minimum in the dispersion loss making these wavelengths the most desirable for operation of the optoelectronic devices. To meet these requirements, lattice-matched III-V compound semiconductor material systems such as $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}/\text{InP}$ for $1.55\text{ }\mu\text{m}$ operation and $\text{In}_{0.74}\text{Ga}_{0.26}\text{As}_{0.58}\text{P}_{0.42}/\text{InP}$ for $1.3\text{ }\mu\text{m}$ operation have been widely used for the fabrication of p-i-n photodiodes,^{99,100} laser diodes, and optical modulators. Of the epitaxial growth technologies used in preparing these lattice-matched III-V material systems, the most serious problem, in terms of controlling the uniform deposition of precise quaternary alloy compositions, is associated with the molecular beam epitaxy (MBE) technique. It is particularly difficult in MBE to precisely control the ratio of As to P in the III-V quaternary alloy system. Furthermore, technology for monolithic integration of the InP based optoelectronic devices on semi-insulating InP substrate material is still far behind that of GaAs IC technology. Therefore, it is highly desirable to develop techniques for the monolithic integration of $\text{In}_x\text{Ga}_{1-x}\text{As}$ photonic devices operating in the 1.0 to $1.6\text{ }\mu\text{m}$ wavelength range with GaAs ICs. The main difficulty, however, with such an approach is that large lattice-mismatches exist between the GaAs and the $\text{In}_x\text{Ga}_{1-x}\text{As}$ materials of interest. Recently, Melman et al.¹⁰¹ have reported the fabrication of devices from strained InGaAs/GaAs quantum-well structures. Unfortunately, the bandgap energy corresponding to the strained InGaAs structure is 0.96 eV (corresponding to $1.29\text{ }\mu\text{m}$) at room temperature, which still does not meet the exact requirement for the $1.3\text{ }\mu\text{m}$ or longer wavelength applications (i.e., $1.55\text{ }\mu\text{m}$).

In this chapter, we report the successful fabrication of a high-quality $\text{In}_{0.4}\text{Ga}_{0.6}\text{As}$ p-i-n photodiode with a peak photoresponse at $1.3\text{ }\mu\text{m}$ grown on a semi-insulating GaAs substrate by the MBE technique, which involves the incorporation of a mul-

tistage strain-relief buffer system. Note that the $\text{In}_{0.4}\text{Ga}_{0.6}\text{As}$ p-i-n photodetector structure reported here has the potential to be monolithically integrated with GaAs electronic devices such as MESFETs, to form OEICs for 1.3 μm applications.

The MBE growth of the multistage strain-relief buffer system that ultimately permits the growth of low-dislocation density, thick $\text{In}_{0.4}\text{Ga}_{0.6}\text{As}$ material on GaAs has been described previously.¹⁰² Briefly, for $\text{In}_x\text{Ga}_{1-x}\text{As}$ alloys with $0 < x < 0.18$, strain due to the lattice-mismatch with GaAs is relieved by plastic deformation of the GaAs substrate in addition to misfit dislocation formation at the hetero-interface, with the $\text{In}_x\text{Ga}_{1-x}\text{As}$ epilayers remaining essentially threading dislocation-free. Dislocations propagate in the GaAs material on account of its lower yield strength. As can be seen from the schematic diagram shown in Fig. 6.1 (a), the first stage of the multistage buffer consists of a 0.2 μm thick $\text{In}_{0.14}\text{Ga}_{0.86}\text{As}$ layer grown on GaAs which was designed to relieve stress in the system developed to this point in the manner discussed above. The subsequent strain-relieving stages incorporated as shown in the schematic diagram were designed in such a way as to promote dislocation propagation primarily in the underlying sacrificial layers, namely, the 0.2 μm thick $\text{In}_{0.14}\text{Ga}_{0.86}\text{As}$ and the 0.2 μm thick $\text{In}_{0.27}\text{Ga}_{0.73}\text{As}$ epilayers. Ultimately, low-dislocation density, thick $\text{In}_{0.4}\text{Ga}_{0.6}\text{As}$ layers can be grown on such a buffer system. It should be noted that the buffer system employed in this work is a slight modification of that reported in Reference 102, however, the basic design philosophy is the same.

6.3 $\text{In}_{0.4}\text{Ga}_{0.6}\text{As}$ p-i-n Photodiode

6.3.1 Device Structure and Design

A schematic diagram of the detector structure is shown in Fig. 6.1(b). A 0.4 μm thick $\text{p}^+ - \text{In}_{0.4}\text{Ga}_{0.6}\text{As}$ layer, a 0.8 μm thick undoped $\text{In}_{0.4}\text{Ga}_{0.6}\text{As}$ layer, and a 0.3 μm thick $\text{n}^+ \text{In}_{0.4}\text{Ga}_{0.6}\text{As}$ layer were grown on top of the buffer system. Based on the -3dB bandwidth calculations by Wake et al.,¹⁰³ it has been shown that the optimum

intrinsic layer thickness is around 0.5 to 0.7 μm for a high-speed top-illuminated $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ p-i-n photodiode. In our design we used an $\text{In}_{0.4}\text{Ga}_{0.6}\text{As}$ active layer thickness of 0.8 μm . Although, its absorption coefficient at 1.3 μm is smaller than that of $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ at 1.55 μm , the value of absorption coefficient is still larger than 10^4 cm^{-1} , which implies that the absorption depth is less than 1 μm . Therefore, using a 0.8 μm undoped $\text{In}_{0.4}\text{Ga}_{0.6}\text{As}$ intrinsic layer is adequate for achieving both the high-speed and high-responsivity operation in this detector. A 1.25 μm deep mesa etch was performed to realize the p-i-n photodiode structure without surface passivation. Metallization for the p^+ and n^+ ohmic contacts was achieved by depositing Cr/Au and Au-Ge/Ni/Au, respectively. Both contacts were then alloyed at 400 $^\circ\text{C}$ for 30 seconds to ensure low contact resistance.

6.3.2 Results and Discussion

The samples of InGaAs/GaAs material obtained are #67, #100 and #102. Parameters of design structure, and growth conditions are listed in Table 6.1. Sample #67 looked mirror-shining, while the samples #100 and #102 showed crosshatched web microstructure under the inspection by conventional metallurgical microscope (see Fig. 6.2). This crosshatched pattern is believed to be the formation of a network of misfit dislocations.¹⁰⁴ In our study, it is found that this network of misfit dislocations seemed electrical inactive. Also the formation of the network reduced the bulk dislocation density. Thus the device properties from the sample #100 and #102 is much better than those in #67.

The typical reverse leakage current obtained for the mesa diodes with 150 μm diameter are $5 \times 10^{-9} \text{ A}$ and 6×10^{-7} at -5 V bias for sample #100 and #102, respectively (see Fig. 6.3(a) and 6.3(b)). Compared with the results of $7 \times 10^{-7} \text{ A}$ at the same bias voltage reported previously from sample #67 (see Figure 6.4), these results show a drastic improvement. The device properties of three samples are compared in Table 6.2.

The best result for the reverse leakage current obtained so far for our mesa-etched $\text{In}_{0.4}\text{Ga}_{0.6}\text{As}$ p-i-n photodiodes with an active area of $2 \times 10^{-4} \text{ cm}^2$ is $5 \times 10^{-9} \text{ A}$ at -5 V (see Fig. 6.5), which corresponds to a current density of 10^{-5} A/cm^2 . This represents an order of magnitude reduction in the dark current over the conventional $\text{In}_{0.53}\text{Ga}_{0.47}\text{As/InP}$ mesa-type photodiode.¹⁰⁵ We believe that the dark current can be further reduced if the detectors were passivated by polyimide or other dielectrics. Based on the C-V measurements, a carrier concentration of $3.5 \times 10^{15} \text{ cm}^{-3}$ was found for the unintentionally-doped $\text{In}_{0.4}\text{Ga}_{0.6}\text{As}$ active layer.

Furthermore, the breakdown voltages of the photodiodes made from those two samples have been obtained and are shown in Fig. 6.6. The breakdown voltage of photodiode from sample #100 is higher than 25 V. Accounting for the thickness of the intrinsic layer ($0.8 \mu\text{m}$), this undoped layer has shown the capability of sustaining an electric-field strength as high as $3 \times 10^5 \text{ V/cm}$ which has fallen into the region for the occurrence of impact ionization. This implies that the film quality of sample #100 is good for design and fabrication of avalanching photodiode.

Figure 6.7 shows a typical spectral response curve of our $\text{In}_{0.4}\text{Ga}_{0.6}\text{As}$ p-i-n photodetector. As shown, the photoresponse peaks at $1.3 \mu\text{m}$, having a responsivity of 0.45 A/W and a quantum efficiency of 42 % at this wavelength. Since a $0.4 \mu\text{m}$ $\text{p}^+-\text{In}_{0.4}\text{Ga}_{0.6}\text{As}$ top layer was used in this detector, a substantial increase in photoresponse is expected for $\lambda \leq 1.3 \mu\text{m}$. The broadening of the spectral response curve around $\lambda = 1.3 \mu\text{m}$ (see Fig. 6.7) may be attributed to the generation of electron-hole pairs by the incident photons absorbed in the p^+ -region.

The bandgap of the $\text{In}_{1-x}\text{Ga}_x\text{As}$ material can be estimated by using the empirical formula in Eq. 2.10. Substituting a value for x of 0.4, the bandgap is found to equal 0.86 eV . This energy corresponds to a cutoff wavelength of $1.44 \mu\text{m}$, which is consistent with our spectral response data shown in Fig. 6.7. At -2.0 V bias, the depletion layer capacitance of the photodiode is equal to 4.0 pF . Assuming that the photogenerated

signal is fed into a $50\ \Omega$ load, the RC time constant of the photodiode will be 200 ps. On the other hand, the free carrier transit time across the depletion region is estimated to be 27 ps, if the hole saturation velocity is assumed equal to 3×10^6 cm/s. Thus, the response speed of our $\text{In}_{0.4}\text{Ga}_{0.6}\text{As}$ p-i-n photodiodes is estimated to be greater than 1 GHz.

6.4 Electrical Characterization of the $\text{In}_{0.4}\text{Ga}_{0.6}\text{As}$ Photodiode

The growth of InGaAs on GaAs is an important technology for on-chip monolithic integration of $1.3 \sim 1.5\ \mu\text{m}$ photonic devices with GaAs LSI electronics. In a p-i-n or MSM photodiode the electron-hole pairs are generated inside the depletion region. Therefore, the generation lifetime and deep-level defects which determine the dark current of the reverse-biased junction are important parameters for determining the performance of such devices. In III-V photodiodes, the main contributions of the dark leakage current are from the bulk defects and surface states. Studies of surface leakage currents in InGaAs/InP photodiodes have been reported by Ducroquet et al.¹⁰⁶ For the $\text{In}_{0.4}\text{Ga}_{0.6}\text{As}/\text{GaAs}$ material system, the deep-level defects are generally higher than those in the lattice-matched InGaAs/InP material system. Thus, the bulk leakage current is expected to be the dominant component in the $\text{In}_{0.4}\text{Ga}_{0.6}\text{As}$ p-i-n photodiode formed on GaAs.

Spiegel and Declerck¹⁰⁷ used a gate-controlled-diode to measure the reverse leakage current for determining the generation lifetime. However, adding gate structure to the planar diode alters the field distribution, and hence the lateral space-charge-region (SCR) width is not identical to the vertical SCR width. In this chapter, we employ a simple differential current and capacitance technique¹⁰⁸ to determine directly the generation lifetime profile in the i-region of an $\text{In}_{0.4}\text{Ga}_{0.6}\text{As}$ p-i-n photodiode on GaAs from the reverse-biased I-V and C-V data. In addition, the DLTS method was employed to determine the defect parameters and generation lifetime in the samples.

6.4.1 Generation Lifetime and Deep Level Defects

The p-i-n photodiode structure used in this study is shown in Fig. 6.1. A $0.4\text{-}\mu\text{m}$ $\text{p}^+\text{-In}_{0.4}\text{Ga}_{0.6}\text{As}$ layer, a $0.8\text{-}\mu\text{m}$ undoped $\text{In}_{0.4}\text{Ga}_{0.6}\text{As}$ layer, and a $0.3\text{-}\mu\text{m}$ $\text{n}^+\text{-In}_{0.4}\text{Ga}_{0.6}\text{As}$ layer were grown on top of the strain-relief buffer layer on a GaAs substrate. A $150\text{ }\mu\text{m}$ diameter mesa structure was formed in the $\text{In}_{0.4}\text{Ga}_{0.6}\text{As}$ p-i-n photodiode without surface passivation. In a p-i-n diode, the total reverse leakage currents can be expressed by⁶⁸

$$I_r(V_r) = A_b q \int_0^{W(V_r)} \frac{n_i}{\tau_g(x)} dx + A_s q n_i S_0 + I_{diff}(V_r) + I_{fe}(V_r) \quad (6.1)$$

where A_b is the area of the bulk space-charge region, A_s is the surface area of the photodiode, and S_0 is the surface generation velocity. In Eq. (1), the total reverse-biased currents consist of (i) bulk generation current, (ii) surface generation current, (iii) diffusion current, and (iv) field enhanced current. The field enhanced current is significant only when V_r is large, which is not the present case. The diffusion current is negligible due to the small intrinsic carrier concentration and thin $\text{In}_{0.4}\text{Ga}_{0.6}\text{As}$ layer. Since, the surface generation current is independent of the bias voltage, its derivative with respect to the biasing voltage can be neglected. From the model given in Reference 109, the generation lifetime profile can be expressed as

$$\tau_g(W) = K \frac{\epsilon_s q n_i A_b^2}{C^n} \frac{dC/dV_r}{dI_r/dV_r} \quad (6.2)$$

where symbols used in Eq. 6.2 have their usual meanings. For one-sided abrupt junction $n=2$, $K=1$, while for linearly graded junction, $n=3/2$, $K=2/3$, etc. In Eq. 6.2, C , dC/dV_r , and dI_r/dV_r are a function of the generation layer width W , and hence the profile of generation lifetime within the i-layer of the photodiode can be determined from the measured quantities in Eq. 6.2.

In an undoped III-V semiconductor, the Shockley-Read-Hall mechanism¹¹⁰ may dominate the carrier generation process of a reverse-biased p-n junction diode. Therefore, by applying this model, the generation lifetime in the i-region of an $\text{In}_{0.4}\text{Ga}_{0.6}\text{As}$

p-i-n photodiode for a single-level generation center, can be expressed as

$$\tau_g = \frac{1}{\sigma_p v_{th} N_T} \exp\left(\frac{E_T - E_i}{kT}\right) + \frac{1}{\sigma_n v_{th} N_T} \exp\left(-\frac{E_T - E_i}{kT}\right) \quad (6.3)$$

where E_T is the trap energy level in the i-region of the diode, N_T is the corresponding electron trap densities, σ_n is the capture cross section of electron, σ_p is the capture cross section of hole, v_{th} is the electron saturation velocity, and E_i is the mid-gap level in the $\text{In}_{0.4}\text{Ga}_{0.6}\text{As}$ photodiode. Since σ_n , N_T and E_T can be obtained from the DLTS measurements, by assuming $\sigma_n = \sigma_p$ the average generation lifetime can be determined.

6.4.2 Experiments and Discussion

The I-V and C-V measurements were performed at room temperature using an HP4140 pA-meter and an HP4280A C-meter. The capacitance vs. temperature measurements for the conventional DLTS technique was carried out between 80 to 300 K using an HP4280A C-meter and an HP8112A pulse generator. Six rate windows between 12.5 s^{-1} and 625 s^{-1} were used for the DLTS measurements. The I-V and C-V curves for a typical $\text{In}_{0.4}\text{Ga}_{0.6}\text{As}$ p-i-n photodiode formed on GaAs are shown in Fig. 6.8. The measured dark current was $5 \times 10^{-9} \text{ A}$ at $V_r = -5 \text{ V}$. The junction capacitance varies from 6 to 4 pF as the reverse bias voltage increases from 0 to -5 V. Data taken from the I-V and C-V measurements were then used in Eq. 6.2 to compute τ_g and its dependence on the distance away from the p-i-n junction interface. The results are shown in Fig. 6.9, which reveals that the closer to the strain-relief buffer interface the small the generation lifetime τ_g is, indicating an increase of the deep-level defects at the buffer layer interface. It was suggested by Matthews et al.¹¹⁰ that the misfit strain induced dislocations in the large lattice constant layers grown on sphalerite type crystals could be Frank-Read centers. The model predicts a gradual reduction of crystal defects as the device quality layer growing front moves away from the heterojunction interface. Our generation lifetime measurement confirms the prediction of this model and gives a quantitative description of the generation lifetime

profile. Similarly, at the p-n junction interface, τ_g is also expected to decrease due to the effect of junction interface states.

Figure 6.10 shows the DLTS spectra (in the inset) and the corresponding Arrhenius plot for determining the energy level of the electron trap and the capture cross section. In the inset of Fig. 6.10, the rate windows R1 through R4 correspond to the emission rates of 12.5, 31.25, 62.5, and 125 s^{-1} , respectively. One dominant electron trap was detected for temperature between 80 to 300 K . The apparent activation energy, E_a , the capture cross section σ , and the trap concentration, N_T were found to be $E_c-0.41$ eV, 1.2×10^{-14} cm^2 , and 6.3×10^{14} cm^{-3} , respectively. By substituting these values into Eq. 6.3, an average generation lifetime, τ_g , was found to be 7×10^{-7} s. This value is a factor of five higher than the value obtained from the differential I-V/C-V technique. This discrepancy may be explained by the fact that there were other shallower defect levels which were not taken into account in our calculations, as clearly shown in Fig. 6.10.

6.5 Conclusion

In summary, we have demonstrated the successful fabrication of a high sensitivity, low dark current, planar $In_{0.4}Ga_{0.6}As$ p-i-n photodiode grown on a semi-insulating GaAs substrate with a peak photoresponse at 1.3 μm wavelength. Our results provide a major step toward the realization of monolithic integration of InGaAs optoelectronic devices with GaAs electronic devices for 1.3 μm fiber optical communications and other OEIC's applications.

We have also studied the physical parameters which affect the reverse leakage current in the $In_{0.4}Ga_{0.6}As$ p-i-n photodiode prepared on GaAs by MBE technique. The differential I-V and C-V technique has been used for determining the generation lifetime profile in an $In_{0.4}Ga_{0.6}As$ p-i-n photodiode. DLTS measurements have also been performed on these devices to obtain the deep-level defects and the average gen-

eration lifetime in the i-region of the device. Good agreement on generation lifetime was obtained from these two characterization techniques.

Table 6.1 Structure parameters and growth conditions for $\text{In}_{0.4}\text{Ga}_{0.6}\text{As}$ materials.

Sample No.	#67	#100	#102																																
Scheme of stress relief buffer structure	<div><div>50 X {<table><tr><td>1.0 μm</td><td>In_{0.40}Ga_{0.60}As</td></tr><tr><td>20 Å</td><td>In_{0.50}Al_{0.40}As</td></tr><tr><td>20 Å</td><td>In_{0.26}Ga_{0.74}As</td></tr></table></div><div>66 X {<table><tr><td>0.2 μm</td><td>In_{0.26}Ga_{0.74}As</td></tr><tr><td>20 Å</td><td>In_{0.36}Ga_{0.64}As</td></tr><tr><td>10 Å</td><td>GaAs</td></tr><tr><td>0.2 μm</td><td>In_{0.14}Ga_{0.86}As</td></tr><tr><td>0.2 μm</td><td>GaAs Buffer</td></tr></table></div></div>	1.0 μm	In _{0.40} Ga _{0.60} As	20 Å	In _{0.50} Al _{0.40} As	20 Å	In _{0.26} Ga _{0.74} As	0.2 μm	In _{0.26} Ga _{0.74} As	20 Å	In _{0.36} Ga _{0.64} As	10 Å	GaAs	0.2 μm	In _{0.14} Ga _{0.86} As	0.2 μm	GaAs Buffer	<div><div>50 X {<table><tr><td>1.0 μm</td><td>In_{0.40}Ga_{0.60}As</td></tr><tr><td>20 Å</td><td>In_{0.52}Ga_{0.47}As</td></tr><tr><td>20 Å</td><td>In_{0.27}Ga_{0.73}As</td></tr></table></div><div>50 X {<table><tr><td>0.2 μm</td><td>In_{0.27}Ga_{0.73}As</td></tr><tr><td>20 Å</td><td>In_{0.40}Ga_{0.60}As</td></tr><tr><td>20 Å</td><td>In_{0.14}Ga_{0.86}As</td></tr><tr><td>0.2 μm</td><td>In_{0.14}Ga_{0.86}As</td></tr><tr><td>0.2 μm</td><td>GaAs</td></tr></table></div></div>	1.0 μm	In _{0.40} Ga _{0.60} As	20 Å	In _{0.52} Ga _{0.47} As	20 Å	In _{0.27} Ga _{0.73} As	0.2 μm	In _{0.27} Ga _{0.73} As	20 Å	In _{0.40} Ga _{0.60} As	20 Å	In _{0.14} Ga _{0.86} As	0.2 μm	In _{0.14} Ga _{0.86} As	0.2 μm	GaAs	Same as #100
	1.0 μm	In _{0.40} Ga _{0.60} As																																	
20 Å	In _{0.50} Al _{0.40} As																																		
20 Å	In _{0.26} Ga _{0.74} As																																		
0.2 μm	In _{0.26} Ga _{0.74} As																																		
20 Å	In _{0.36} Ga _{0.64} As																																		
10 Å	GaAs																																		
0.2 μm	In _{0.14} Ga _{0.86} As																																		
0.2 μm	GaAs Buffer																																		
1.0 μm	In _{0.40} Ga _{0.60} As																																		
20 Å	In _{0.52} Ga _{0.47} As																																		
20 Å	In _{0.27} Ga _{0.73} As																																		
0.2 μm	In _{0.27} Ga _{0.73} As																																		
20 Å	In _{0.40} Ga _{0.60} As																																		
20 Å	In _{0.14} Ga _{0.86} As																																		
0.2 μm	In _{0.14} Ga _{0.86} As																																		
0.2 μm	GaAs																																		
Substrate temp. for growing top buffer layer	450° C	370° C	350° C																																

Table 6.2 Device and material properties of the $\text{In}_{0.4}\text{Ga}_{0.6}\text{As}$ photodiodes.

Sample No.	#67	#100	#102
leakage current at -5 V	$7 \times 10^{-7} \text{ A}$	$5 \times 10^{-9} \text{ A}$	$6 \times 10^{-7} \text{ A}$
breakdown voltage ($I_D > 20 \text{ A}$)	2.5 V	25 V	8 V
zero-bias capacitance	---	5.9 pF	7.8 pF
electron mobility cm^2/Vs	2200	4800	4300
dislocation density cm^{-2}	1×10^8	2×10^6	1×10^7

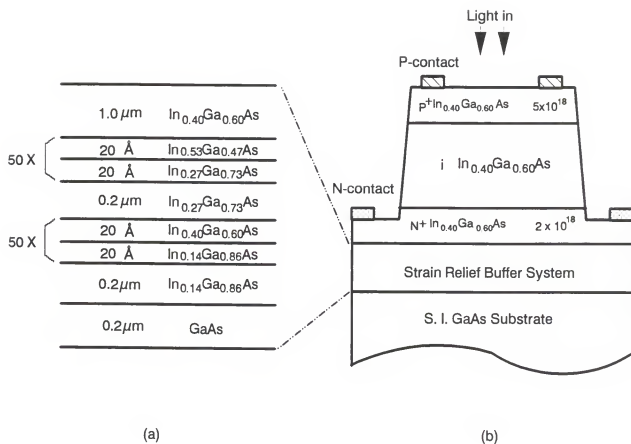
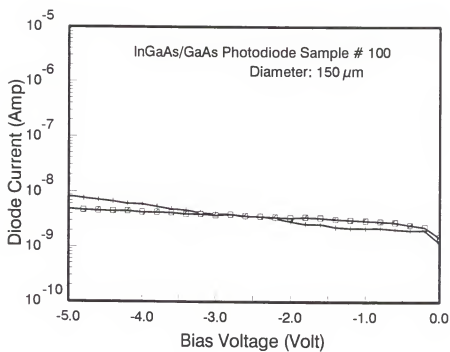


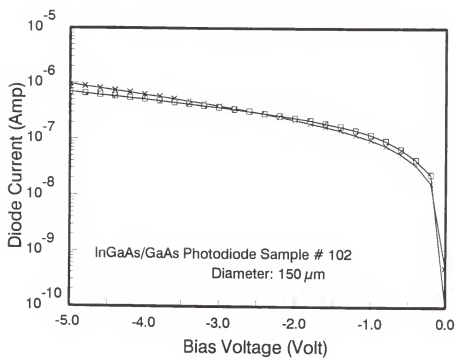
Figure 6.1 Schematic diagram of an $\text{In}_{0.4}\text{Ga}_{0.6}\text{As}$ p-i-n photodiode. (a) A detailed MBE growth scheme of the $\text{In}_{0.4}\text{Ga}_{0.6}\text{As}/\text{GaAs}$ p-i-n layer structure with the strain-relief buffer system; (b) the cross section view of the mesa-etched p-i-n photodiode.



Figure 6.2 Top surface of the mesa diode; the crosshatched pattern can be clearly seen. It is believed that some of the mismatch strain has been relieved by the formation of misfit dislocation.



(a)



(b)

Figure 6.3 Typical reverse leakage current for sample (a) #100 and (b) #102.

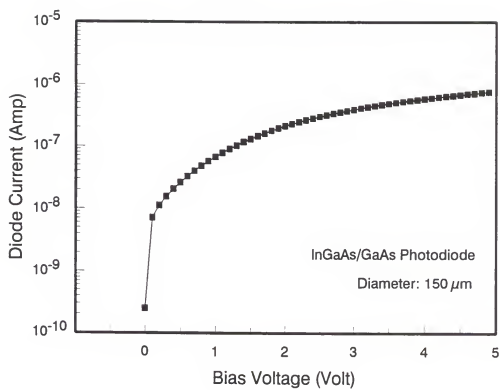


Figure 6.4 Typical reverse leakage current for sample #67.

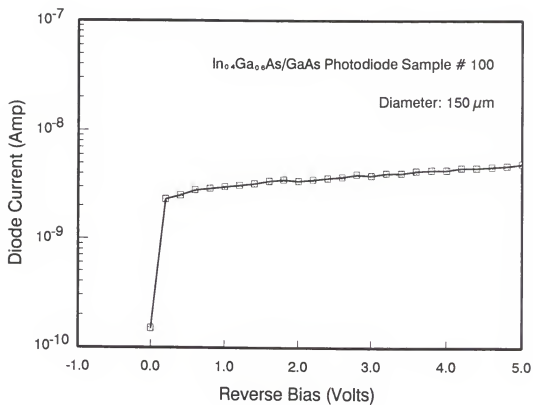
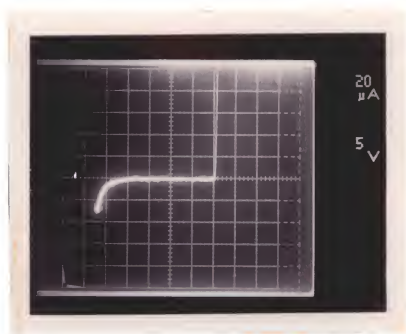
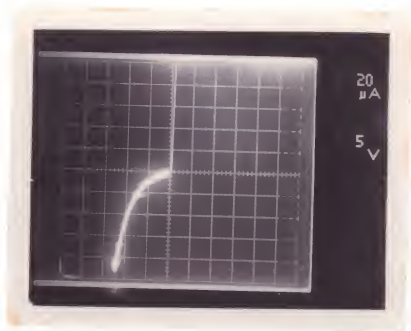


Figure 6.5 Reverse dark current of the $\text{In}_{0.4}\text{Ga}_{0.6}\text{As}$ p-i-n photodiode. The active area of the mesa-etched photodiode is $2 \times 10^{-4} \text{ cm}^2$.



Sample
100



Sample
102

Figure 6.6 Breakdown voltage of photodiodes sample #100 and #102.

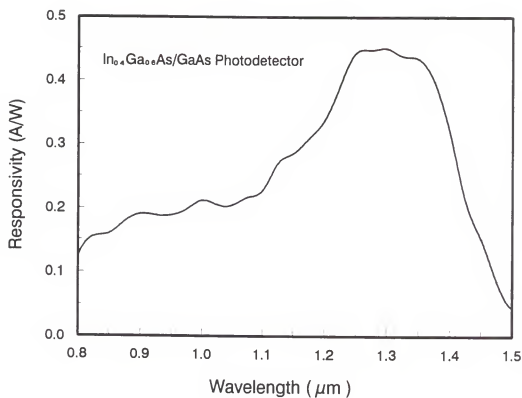


Figure 6.7 The spectral response of an $\text{In}_{0.4}\text{Ga}_{0.6}\text{As}$ p-i-n photodiode. Peak response of the photodiode occurs at 1.3 μm wavelength with a responsivity of 0.45 A/W and a quantum efficiency of 42%.

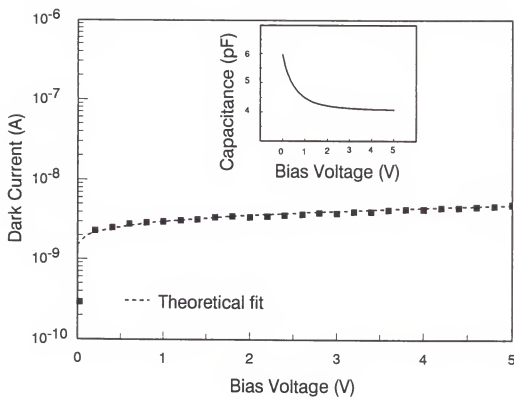


Figure 6.8 Typical I-V and C-V curves of the $\text{In}_{0.4}\text{Ga}_{0.6}\text{As}$ p-i-n photodiode formed on GaAs.

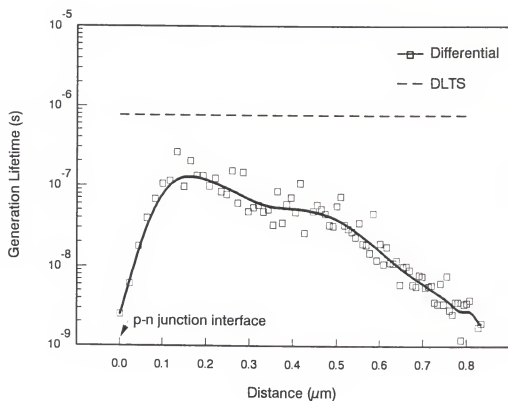


Figure 6.9 The generation lifetime profile in the i-region of an $\text{In}_{0.4}\text{Ga}_{0.6}\text{As}$ p-i-n photodiode. The dash line represents the average generation lifetime obtained by the DLTS method.

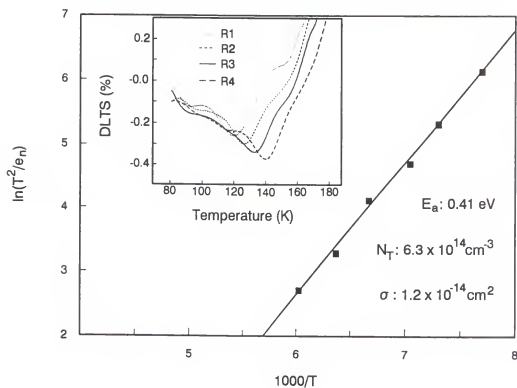


Figure 6.10 The DLTS thermal scans for different rate windows and the corresponding Arrhenius plot for an $\text{In}_{0.4}\text{Ga}_{0.6}\text{As}$ p-i-n photodiode grown on GaAs by MBE technique.

CHAPTER 7

CONCLUSIONS AND RECOMMENDATIONS

Several conclusions can be drawn from the research work described in this dissertation which are summarized as follows:

- Development of a high performance $\text{In}_{0.4}\text{Ga}_{0.6}\text{As}$ photodiode grown on GaAs substrate for $1.3\ \mu\text{m}$ wavelength detection. The device showed a low dark current of $5 \times 10^{-9}\ \text{A}$ at $-5\ \text{V}$. Compared with other recent works in the same area, this is a significant achievement. The quantum efficiency and responsivity of the detector at $1.3\ \mu\text{m}$ wavelength are 42% and $0.45\ \text{A/W}$, respectively. The electrical characterization of the device has also been performed. A generation lifetime profile was obtained by the I-V/C-V differential technique. An electron trap near the midgap of $\text{In}_{0.4}\text{Ga}_{0.6}\text{As}$ semiconductor was detected by a DLTS measurement.
- Development of a high speed GaAs Schottky barrier photodiode prepared on Si substrate for $0.84\ \mu\text{m}$ wavelength detection. The device showed good responsivity of $0.25\ \text{A/W}$. Measured bandwidth of the device was $5\ \text{GHz}$. A sub-nanoampere ($9 \times 10^{-10}\ \text{A}$) reverse leakage current for the device has been achieved.
- Effective improvement of the performance of the GaAs Schottky barrier photodiode by insertion of a multi-layer reflector of 14 periods of $\text{GaAs}/\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$ structure into the ohmic contact side of the detector. The multi-layer reflector was designed by the scattering matrix technique. An increase of 30% responsivity at $0.84\ \mu\text{m}$ wavelength has been obtained in this study.

- Design and analysis of a multi-gigahertz preamplifier by using the state of art double-poly self-aligned Si BJT technology. Simulation of the circuit was performed by ASTAP circuit simulator with a $0.4 \times 0.8 \mu\text{m}^2$ n-p-n transistor model widely used in the industry. Depending on the values of the photodetector capacitance, bandwidth between 2.5 to 7 GHz has been obtained from the simulation. Assuming a 70% quantum efficiency for the photodetector, a receiver sensitivity of -28 dBm at 10^{-9} bit-error-rate has been estimated. The dynamic range of the preamplifier was found to be 45 dB.
- Development of a high-gain $1.0 \mu\text{m}$ gate length MESFET on Si substrate. In the AC measurement, a cutoff frequency of 11 GHz has been obtained. The device has also been wired as high impedance amplifier and hybrid-integrated with a Schottky barrier photodiode on a ceramic substrate. An impulse response of 380 ns (FWHM) for the receiver has been obtained.

From the above conclusions, it has been demonstrated that a high sensitivity photoreceiver, one of the most important elements in the OEIC family, has been successfully developed on the lattice mismatched material systems, i.e., GaAs-on-Si for 0.8 to $0.9 \mu\text{m}$ wavelength and InGaAs-on-GaAs for 1.3 to $1.55 \mu\text{m}$ wavelength detection. To further study in this area, the following suggestions are recommended:

- Monolithic integration of an InGaAs photodiode with a GaAs MESFET preamplifier should be pursued. This study will reveal the interconnect ability between devices made by InGaAs and GaAs materials.
- High indium content InGaAs-on-GaAs-on-Si or InGaAs directly on Si material system is worthy of exploring since Si IC is by far the most mature technology in the semiconductor industry. The commercialization of OEIC is unavoidably needed to be integrated with Si circuitry.

- Integration of passive optical elements, such as waveguide and 3-dB coupler etc., into the chip with electronic circuitry needs to be studied further. It is even more so in the case of lattice mismatched material systems since it has the advantage of large refraction index selection among the Si, SiO_x , GaAs, AlGaAs, and InGaAs materials.

REFERENCES

- [1] T. V. Moui, J. Lightw. Technol. **LT-2**, 243 (1984).
- [2] S. Margalit and A. Yariv in "Semiconductor and Semimetal," Vol. 22, pt. E, edited by R. K. Willardson and A. C. Beer, Academic Press, Chapter 2, New York (1985), p. 203.
- [3] S. R. Forrest, IEEE Trans. Electron Devices, **ED-32**, 2640 (1985).
- [4] O. Wada, T. Sakurai, and T. Nakagami, IEEE J. Quan. Elec. **QE-22**, 805 (1986).
- [5] W. J. Tomlinson and C. A. Brackett, IEEE Proc., **75**, 1512 (1987).
- [6] M. Dagenais, R. F. Leheny, H. Temkin, and P. Bhattacharya, J. Lightw. Technol., **LT-8**, 846 (1990).
- [7] T. Horimatsu and M. Sasaki, J. of Lightwave Technol., **LT-7** (11), 1612 (1989).
- [8] J. K. Butler, A. R. Galawa, R. J. Phelen, T. C. Harman, A. J. Stranes and R. H. Rediker, Appl. Phys. Lett., **5**, 75 (1964).
- [9] H. C. Casey, Jr., and M. B. Panish, "Heterostructure Lasers," Academic Press, New York (1978).
- [10] T. P. Persall, B. I. Miller, R. J. Capik, and K. J. Bachmann, Appl. Phys. Lett., **28**, 449 (1976).
- [11] F. C. Frank, and J. H. Van der Merwe, Proc. Roy. Soc. London, **198**, 216 (1949).
- [12] J. W. Matthews, and A. E. Blakeslee, J. Cryst. Growth, **29**, 273 (1975).
- [13] M. Shimizu, K. Suwara, and T. Sakurai, J. Jpn. Ass. Cryst. Growth, **13**, 253 (1986).
- [14] J. W. Lee in "GaAs and Related Compounds 1986," edited by W. T. Lindley, Institute of Physics, Bristol, England, (1986), p. 111.
- [15] T. Nishioka, Y. Itoh, A. Yamamoto, and M. Yamaguchi, Appl. Phys. Lett., **51**, 1928 (1987).
- [16] M. Yamaguchi, A. Yamamoto, M. Tachikawa, Y. Itoh. and M. Sugo, Appl. Phys. Lett., **53**(23), 2293 (1988).

- [17] S. D. Personick, Bell Syst. Tech. J., **52**, 843 (1973).
- [18] S. D. Personick, Proc. IEEE, **65**, 1670 (1977).
- [19] D. R. Smith and I. Garret, Opt. Quantum Electron., **10**, 211 (1978).
- [20] K. Ogawa, IEEE J. Selected Areas Commun., **SAC-1**, 524 (1983).
- [21] S. D. Personick, Proc. IEEE, **68**, 1254 (1980).
- [22] D. L. Rogers, A. X. Widmer and J. Mosley, IBM Research Report RC10286, Dec. 1983.
- [23] Y. Imai, N. Kato, K. Ohivada, and T. Sugeta, IEEE Trans. Microwave Theory Technol., **MTT-33**, 686 (1985).
- [24] R. A. Minasian, J. Lightwave Technol., **LT-5**(3), 373 (1987).
- [25] R. G. Smith and S. D. Personick, in "Semiconductor Devices for Optical Communication," 2nd Edition, edited by H. Kressel, Springer-Verlag, Berlin, Chapter 4, (1987), p. 89.
- [26] M. Brain, T. P. Lee, J. Lightwave Technol., **LT-3**(6), 1285 (1985).
- [27] C. P. Lee, S. Margalit, I. Ury, and A. Yariv, Appl. Phys. Lett., **32**, 806 (1977).
- [28] R. F. Legemy, R. E. Nahory, M. A. Pollack, A. A. Ballman, E. D. Beebe, J. C. Dewinter, and R. J. Martin, Electron. Lett., **16**, 353 (1980).
- [29] S. Mivra, O. Wada, H. Hamaguchi, M. Ito, M. Makinchi, K. Nakai, and T. Sakurai, IEEE Electron Device Lett., **EDL-4**, 375 (1983).
- [30] R. M. Kolbas, J. Abrokwhah, J. K. Carney, D. H. Bradshaw, B. R. Elemer, and J. R. Biard, Appl. Phys. Lett., **43**, 821 (1983).
- [31] R. S. Sussmann, R. M. Ash, A. J. Moseley, and R. C. Goodfellow, Electron. Lett., **22**, 593 (1985).
- [32] O. Wada, M. Makiuchi, H. Hamaguchi, T. Kumai, and T. Mikawa, J. Lightwave Technol., **LT-9**(9), 1200 (1991).
- [33] M. Ito, O. Wada, K. Nakai, and T. Sakwai, IEEE Electron Device Lett., **EDL-5**(12), 531 (1984).
- [34] B. J. Van Zeghbroeck, C. Harder, J. M. Halbout, H. Jäckel, H. Meier, W. Patrick, P. Vettiger and P. Wolf, Proc. Intl. Electronic Devices Meeting, Washington, DC, (1987), p. 229.
- [35] O. Wada, Proc. Intl. Electronic Devices Meeting, Washington, DC, (1987), p. 225.

- [36] D. L. Rogers, Proc. Pieosecond Elect. and Optoelectron., **4**, 184 (1989).
- [37] J. F. Ewen, K. P. Jackson, R. S. Bates and E. B. Flint, J. Lightwave Technol., **LT-9**(12), 1755 (1991).
- [38] H. M. Rein, IEEE Solid-State Circuits, **SSC-23**, 664 (1988).
- [39] H. Hamano, T. Yamamoto, I. Amemiya, T. Touge, and M. Matsuda in ISSCC'88 Dig. Tech. Papers, San Francisco, CA, (1988), p. 18.
- [40] S. Fujita, T. Suzuki, A. Matsuoka, S. Miyazaki, T. Torikai, T. Nakata, M. Shikada, Electron. Lett., **26**, 175 (1990).
- [41] R. P. Gale, J. C. C. Fan, B-Y. Tsaur, G. W. Turner, and F. M. Davis, IEEE Electron Device Lett., **EDL-2**, 169 (1981).
- [42] T. H. Winghorn, G. M. Metze, B. Y. Tsaur, and J. C. C. Fan, Appl. Phys. Lett., **45**, 309 (1984).
- [43] T. Ishida, T. Nonaka, C. Yamaguchi, Y. Kwarada, Y. Sarro, M. Akiyama, and K. Kaminishi, IEEE Trans. Electron Devices, **TED-32**, 1037 (1985).
- [44] T. H. Winghorn and G. M. Metze, Appl. Phys. Lett., **47**, 1031 (1985).
- [45] M. Razeghi, P. Maulel, M. Deffon, F. Omnes and O. Acher, Proc. ECOC'88, Brighton, UK, pt. 2, (1988), p. 74.
- [46] N. Chand, J. Allam, J. M. Gibson, F. Capasso, F. Beltram, A. T. Macrander, A. L. Hutchinson, L. C. Hopkins, C. G. Bethea, B. F. Levine, and A. Y. Chao, J. Vac. Sci. Technol., **B5**, 822 (1987).
- [47] J. W. Adkisson, T. I. Kamins, S. M. Koch, J. S. Harris Jr., S. J. Rosner, K. Nanka, and G. A. Reid, Mat. Res. Soc. Sym. Proc., **116**, 99 (1988).
- [48] J. Paslaski, H. Z. Chen, H. Morkoc, and A. Yariv, Appl. Phys. Lett., **52**, 1410 (1988).
- [49] J. D. More, R. Mariella, G. D. Anderson, and R. W. Dutton, IEEE Electron Device Lett., **10**, 7 (1989).
- [50] R. E. Nahory, M. A. Pollack, and J. C. DeWinter, Appl. Phys. Lett., **25**(3), 146 (1974).
- [51] M. J. Ludowise, W. T. Dietze, C. R. Lewis, M. D. Kamras, N. Holongak, Jr., B. K. Fuller and M. A. Nixon, Appl. Phys. Lett., **42**, 487 (1983).
- [52] M. Razeghi, J. Ramdani, H. Verrielle, D. Decoster, M. Coustant, and J. Vanbremeersch, Appl. Phys. Lett., **49**, 215 (1986).
- [53] P. D. Hodson, R. H. Wallis, J. I. Davies, Electron. Lett., **23**, 273 (1987).

- [54] A. G. Dentai, J. C. Campbell, C. H. Joyner, and G. J. Qua, *Electron. Lett.*, **23**, 38 (1987).
- [55] D. L. Rogers, J. M. Woodall, G. D. Pettit, and D. McInturff, *IEEE Electron Device Lett.*, **EDL-9**(10), 515 (1988).
- [56] J. Frey and D. E. Ioannou, in "Measurement of High-Speed Signal in Solid State Devices," edited by R. B. Marcus, Academic Press, New York, Chapter 1 (1990), p. 3.
- [57] B. R. Nag, "Theory of Electrical Transport in Semiconductors," Pergamon Press, Oxford, England (1972).
- [58] R. H. Bube, "Electronic Properties of Crystalline Solids." Academic Press, New York (1974).
- [59] S. Adachi, *J. Appl. Phys.*, **53**, 8775 (1982).
- [60] S. F. Fang, K. Adomic, S. Iyer, H. Morkoc, and H. Zabel. *J. Appl. Phys.* **68**(7), 31 (1990).
- [61] F. H. Pollak and M. Cadona, *Phys. Rev.*, **172**, 816 (1968).
- [62] A. Gavin and M. Cardona, *Phys. Rev.*, **B1**, 672 (1970).
- [63] T. P. Lee, T. Y. Li, in "Optical Fiber Communications," edited by S. E. Miller and A. G. Chynoweth, Academic Press, New York, Chapter 18, (1979).
- [64] S. S. Li, "Physical Electronics," in press, Plenum, New York.
- [65] O. R. Clark Jones, D. Goodwin, and G. Pullan, "Standard procedures for testing infrared detectors and for describing their performance." AD No. 257597, Office of Defense and Development Research and Engineering, Department of Defense, Washington DC, (1960), pp. 1-45.
- [66] G. Lucovsky and R. B. Emmons, *Appl. Opt.*, **4**, 697 (1965).
- [67] R. S. Muller and T. I. Kamin, "Device Electronics for Integrated Circuits," John Wiley & Sons, New York (1986).
- [68] S. M. Sze, *Physics of Semiconductor Devices*, John Wiley & Sons, New York (1981).
- [69] G. W. Turner, G. M. Metzger, V. Diadrak, B. Y. Tsaur and H. W. Le, *IEDM, Tech. Dig.*, 468 (1985).
- [70] Y. C. Kao, H. Y. Liu, H. L. Tsai, W. M. Duncan, T. S. Kim, and H. Schichijo, *J. Vac. Sci. Technol.*, **B8**, 250(1990).

- [71] N. Chand, R. Fischer, A. M. Sergent, D. V. Lang, S. J. Pearton, and A. Y. Chao, *Appl. Phys. Lett.*, **51**, 1013 (1987).
- [72] W. Shockley, Rep. Al-TDR-64-207 (Air Force Atomic Laboratory, Wright Patterson AFB, OH, 1964).
- [73] J. E. Bowers and C. A. Burrus, *J. Lightwave Technol.*, **LT-5**, 1339 (1987).
- [74] A. Chin and T. Y. Chang, *J. Vac. Sci. Technol.*, **B8**(2), 339 (1990).
- [75] M. S. Ünlü, K. Kishino, J. I. Chyi, L. Arsenault, J. Reed, S. Noor Mohammad and H. Morkoc, *Appl. Phys. Lett.*, **57**(8), 750 (1990).
- [76] R. Kuchibhotla, A. Spinivason, J. C. Campbell, C. Lei, D. G. Deppe, Y. S. He, and B. G. Streetman, *IEEE Photonics Technol. Lett.*, **3**(4), 354 (1991).
- [77] A. G. Dentai, R. Kuchibhotla, J. C. Campbell, C. Tsai, and C. Lei, *Electron. Lett.*, **27**(23), 2125 (1991).
- [78] S. Datta, "Quantum Phenomena," Addison-Wesley, New York (1989).
- [79] D. H. Lee, S. S. Li, and N. G. Paulter, *IEEE J. Quan. Elec.*, **25**, 858 (1989).
- [80] S. Moustakas, J. L. Hullett, and T. D. Styhens, *Optical and Quantum Electronics*, **14**, 57 (1982).
- [81] J. E. Goell, *Bell Syst. Tech. J.*, **53**, 624 (1974).
- [82] P. K. Range, *IEEE Trans. Commun.*, **COM-24**, 413 (1976).
- [83] R. C. Hooper, D. R. Smith, K. Ahmad, D. Jenkins, A. W. Mabbitt, and R. Nicklin, "PIN-FET hybrid optical receivers for longer wavelength optical communications systems," in *Proc. 6th European Conf. Optical Commun.*, Sept. 1980, p. 222.
- [84] Y. Ueno, Y. Ohgushi, and A. Abe, "A 40 Mb/s and a 400 Mb/s repeater for fiber optic communications," in *Proc. 1st European Conf. Optical Commun.*, Sept. 1975, p. 147.
- [85] J. L. Hullett and T. V. Muoi, *IEEE Trans. Commun.*, **COM-24**, 1180 (1976).
- [86] R. G. Smith C. A. Brackett, H. W. Reinbold, *Bell Syst. Tech. J.*, **57**, 1809 (1978).
- [87] R. T. Unwin, *Optical and Quantum Electron*, **14**, 61 (1982).
- [88] S. Moustakas, J. L. Hullett, and T. D. Stephens, *Optical and Quantum Electron*, **14**, 57 (1982).

- [89] M. Ohara, Y. Akazawa, N. Ishihara, and S. Konaka, IEEE J. Solid-State Circuits, **SE19**(4), 491 (1985).
- [90] R. G. Meyer and R. A. Blauschild, IEEE J. Solid-State Circuits, **SC-21**(4), 530 (1986).
- [91] J. L. Hullett and T. V. Muoi, IEEE Trans. Commun. **COM-24**, 1180 (1976).
- [92] Tze-Chiang Chen, K. Y. Toh, J. D. Creeler, Jamies Warnock, Pong-Fei Lu, Denny D. Tang, G. P. Li, Ching-Te Chuang and Tak H. Ning, IEEE Electron Device Lett., **EDL-10**(8), 364 (1989).
- [93] T. H. Ning and D. D. Tang, Proc. IEEE, **74**, 1669 (1986).
- [94] L. Treitinger and M. Miura-Mattausch, ed., "Ultra fast silicon bipolar technology," Berlin, Springer (1988).
- [95] S. Konaka, E. Yamamoto, K. Sakuma, Y. Amemiya, and T. Sakai, IEEE Trans. Electron Devices, **36**, 1370 (1989).
- [96] C. Snapp, "Practical silicon bipolar IC for RF, microwave, and lightwave system applications," presented at WESCON'89, San Francisco, CA (1989).
- [97] P. R. Gray and R. G. Meyer, "Analysis and design of analog integrated circuits," New York, John Wiley & Sons (1977).
- [98] H. Shichijo, R. Matyi, A. H. Taddiken, and Y. C. Kao, IEEE Trans. on Electron Devices, **37**(3), 548 (1990).
- [99] H. T. Griem, S. Ray, J. L. Freeman, and D. L. West, Appl. Phys. Lett., **56**, 1067 (1990).
- [100] C. E. Hurwitz and J. J. Hsieh, Appl. Phys. Lett., **32**, 487 (1978).
- [101] P. Melman, B. Elman, C. Jagannath, E. S. Koteles, A. Silletti, and D. Dugger, Appl. Phys. Lett., **55**, 1436 (1989).
- [102] P. Ribas, V. Krishnamoorthy, and R. M. Park, Appl. Phys. Lett., **57**, 1040 (1990).
- [103] D. Wake, L. C. Blank, R. H. Walling, and I. D. Henning, IEEE Electron Device Lett., **EDL-9**, 226 (1988).
- [104] T. P. Pearsall, in "Strained-Layer Superlattices: Physics," Vol. 32 of Semiconductor and Semimetal, edited by R. K. Willardson and A. C. Beer, Academic Press, New York. Chapter 1 (1990).
- [105] S. R. Forrest, I. Camlibel, O. K. Kim, H. J. Stocker, and J. R. Zuber, IEEE Electron Device Lett., **EDL-2**, 283 (1981).

- [106] F. Ducroquet, G. Guillot, J. C. Renaud, and A. Nouailkat, SPIE, Vol. 1144 Indium Phosphide and Related Material for Advanced Electronic and Optical Devices, Bellingham, Washington (1989), p. 180.
- [107] J. van der Spiegel and G. J. Declerck, Solid-State Electron., **24**, 869 (1981).
- [108] H. S. Chen, F. T. Brady, S. S. Li, Wade A. Krull, Elec. Dev. Lett., **EDL-10**(11), 496 (1989).
- [109] D. K. Schroder, "Semiconductor material and device characterization," John Wiley & Sons, New York (1990).
- [110] J. W. Matthews, S. Mader, and T. B. Light, J. Appl. Phys., **41**(9), 3800 (1970).

BIOGRAPHICAL SKETCH

Andrew Yen-Chang Tzeng was born in Taichung, Taiwan, in 1952. He received a B.S. degree in physics from the Chung-Cheng Institute of Technology, Taoyuan, Taiwan, in 1974 and an M.S. degree in electrical engineering from the University of Florida, Gainesville, Florida, in 1986.

In 1977, he joined the research staff of the Chung-Shan Institute of Science and Technology. From 1977 to 1982 his research area was in the development of low cost Si solar cells and semiconductor material preparation. Then he joined the High-Voltage Research Group of the same institute and worked on the transient electromagnetic pulse study. In 1986, after a two-year leave of absence to study at the University of Florida, he resumed his research work at the institute as the group leader of the High-Voltage Research Group for two years. Then, he returned to the University of Florida in 1988 to study in the optoelectronic area. In 1991, during his Ph.D. study, he was a co-op student at IBM T. J. Watson Research Center, where he was involved in the design and characterization of advanced communication circuits. After his graduation, he will resume his research work at the Chung-Shan Institute as an associate scientist. His research interests include the development of a high-speed photodetector and OEIC, MMIC design, semiconductor device characterization, and electromagnetic compatibility.

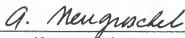
Mr. Tzeng is a member of IEEE, Eta Kappa Nu, and the Association of Old Crows.

I certify that I have read this study and that in my opinion it conforms to acceptable standards of scholarly presentation and is fully adequate, in scope and quality, as a dissertation for the degree of Doctor of Philosophy.



Sheng S. Li, Chairman
Professor of Electrical Engineering

I certify that I have read this study and that in my opinion it conforms to acceptable standards of scholarly presentation and is fully adequate, in scope and quality, as a dissertation for the degree of Doctor of Philosophy.



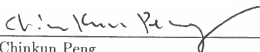
Arnost Neugroschel
Professor of Electrical Engineering

I certify that I have read this study and that in my opinion it conforms to acceptable standards of scholarly presentation and is fully adequate, in scope and quality, as a dissertation for the degree of Doctor of Philosophy.



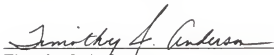
Gys Bosman
Professor of Electrical Engineering

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Chinkun Peng
Assistant Professor of Electrical
Engineering

I certify that I have read this study and that in my opinion it conforms to acceptable standards of scholarly presentation and is fully adequate, in scope and quality, as a dissertation for the degree of Doctor of Philosophy.



Timothy J. Anderson
Professor of Chemical Engineering

This dissertation was submitted to the Graduate Faculty of the College of Engineering and to the Graduate School and was accepted as partial fulfillment of the requirements for the degree of Doctor of Philosophy.

August 1992


fa Winfred M. Phillips
Dean, College of Engineering

Madelyn M. Lockhart
Dean, Graduate School